Estd-1984

KUMARAGURU COLLEGE OF TECHNOLOGY
COIMBATORE – 641 006

ISO 9001:2000 Certified

QUESTION BANK

UNIT I

PART A

1. Convert $(100001110.010)_2$ to a decimal number.
2. Find the canonical SOP for the function f (x_1, x2, x3) = $x_1 + \overline{x_2}\, x_3$
3. State Absorption & De-Morgan's law.
4. Simplify the given Boolean expression Y= ABC + ABC+ABC+ABC.
5. What is prime implicant?
6. Define Min term and Max term.
7. Convert $(10010010)_G$ to binary number.
8. Convert $(1021)_3$ to base 5 Number.
9. Subtract the unsigned number $(10100)_2$ from $(11011)_2$ using one complement and twos complement.
10. Convert $(2120122)_3$ to base 9.
11. State Commutative and Associative Law.
12. Define Canonical form. Express F = XZ' + ZY in a canonical SOP form.
13. Classify Binary Codes.
14. Convert Gray code 101011 into its binary equivalent.
15. Convert $(975)_{10}$ to binary by first converting to octal.
16. Write the truth table for EX-OR Gate.
17. Solve the given expression using Consensus Theorem.

    A'B' + AC + BC' + AB
18. Name the two universal gates.
19. State Distributive and Associative law.
20. How do you implement Y= A + B using a 3 input OR gate?

21. Develop a circuit for the given Boolean Expression using only NAND gates.

$$Y = (A + C)(B' + D)$$

22. Implement AND and OR using NAND gates.

23. Prove the following theorems algebraically.

$$AB + BC + CA = (A + B)\,(B + C)\,(C + A)$$

24. Realize XOR function using only NAND gates.

25. State Duality Theorem.

26. Give some rules in Boolean algebra.

27. How many bits are required to represent the decimal numbers in the range from

    0 – 999 using binary numbers?

PART B

1. Simplify the following Boolean function by using tabulation method.

$$F(A,B,C,D) = \Sigma\,(0,1,4,6,7,8,9,10,11,15)$$

2. Simplify the given Boolean function using 5-variable K-map method.

$$F(V,W,X,Y,Z) = \Sigma\,(1,3,5,6,8,9,13,14,16,21,25,28,31) + \Sigma\,d\,(4,18,23,29)$$

3. Using the k-map method, simplify the Boolean function & obtain minimal

   POS expression $Y = \Sigma\, m\,(0,2,3,6,7) + \Sigma\, d\,(8,10,11,15)$

4. (i) Plot the logical expression A'B'CD + AB'C'D + A'BC + AB' on a 4-variable K-map. Obtain the simplified expression from the map.

   (ii) Obtain the minimal SOP expression for the function.

$$Y = \Sigma\, m\,(1,5,7,13,14,15,17,18,21,22,25,29) + \Sigma\, d\,(6,9,16,23,30)$$

5. Give three possible ways to express the following Boolean functions with minimum literals.

$$F = A'B'D' + AB'CD' + A'BD + ABC'D$$

6. Using the k-map method, simplify the Boolean function & obtain minimal POS expression $Y = \Sigma\, m\,(0,2,3,6,7) + \Sigma\, d\,(8,10,11,15)$

7. Explain how the addition and subtraction can be performed with 1's and 2's complement representations with suitable examples?

8. Reduce the following expressions using K Map.

   F(P,Q,R,S) = ∑m (0,1,4,8,10,11,20,22,24,25,26) + d(0,12,16,17)

   F(A,B,C,D) = ∑m (0,1,4,8,10) + D(2,11)

   F(A,B,C,D) = ∏M (0,2,4,10,11,14,15)

   F(A,B,C,D) = ∑M (4,5,6,7,8,12,13) + d (1,15)

9. Simplify the following 5 variable Boolean expression using Quine McClusky Method.

   F = ∑m (0,1,9,15,24,29,30) + d (8,11,31)

   F = ∑m (2,3,8,9,10,12)

   F = ∑m (0,2,3,6,7,8,9,10,13)

   F = ∑m (0,1,2,3,4,7,9,10)

   F = ∑m (3,4,5,7,9,13,14,15)

10. Reduce the following functions to its minimum sum of products form.

    Y = A'B'C'D' + ABCD' + AB'CD + AB'C'D + ABC'D' + A'B'CD + A'B'C'D'

    Y = A'B'C'D + A'BC'D + A'BCD + A'BCD' + ABC'D' + ABC'D + ABCD

    Y = AB'C + A'B'C + A'BC + AB'C' + A'B'C'

11. Simplify the following Boolean functions.

    F(A,B,C,D,E) = ∑m (0,5,6,8,9,10,11,16,20,25,26,27,29,31)

    F(A,B,C,D,E) = ∑m (0,2,4,6,9,11,13,15,17,21,25,27,29,31)

    F(A,B,C,D,E,F)=∑m (0,5,7,8,9,12,13,23,24,25,28,29,37,40,42,44,46,55,56,57,60,61)

UNIT II

PART A

1. What is de-multiplexer?
2. Distinguish between MUX & decoder.
3. Implement the following function using MUX.

   F (A, B, C) = Σ (1,3,5,6)
4. What are the applications of decoder?
5. What is a comparator?
6. What is a decoder? Give any one example.
7. Implement the function 4-1 multiplexer using 2-1 multiplexer.
8. Distinguish between a multiplexer and a decoder.
9. Describe the truth table of a half adder? What kind of logic circuit can be used to produce the sum and the carry outputs?
10. Implement the function Y = AB’ + A’B using only NOR gates.
11. Give the logical expression for sum and carry for a half adder.
12. Give the logical expression for sum and carry for a full adder.
13. Give the logical expression for difference and borrow for a half subtractor.
14. Give the logical expression for difference and borrow for a full subtractor.
15. Draw the block diagram of n – bit comparator.
16. What is a code converter?
17. Realize the AND function using 2:1 MUX.
18. List some major applications of multiplexer.
19. What is a priority encoder?
20. What do you mean by a comparator? Give its conditions.
21. Differentiate encoder and decoder.

22. What is an ALU?
23. Name the various operations that can be carried out using the ALU.
24. Draw the circuit diagram of a 3 to 8 Decoder.
25. Implement a full adder with two 4 X 1 multiplexer.
26. Draw the block diagram of a combinational logic circuit.
27. Name all the logic gates used to design a logic circuit.

PART B

1. Explain full adder with truth table and logic circuit.
2. Explain full subtractor with truth table and logic circuit.
3. Explain 2 bit comparator with truth table and logic circuit.
4. Design a BCD to gray code converter.
5. Design a BCD to binary converter.
6. Design a binary to BCD converter.
7. Design a gray code to BCD converter.
8. Design a BCD to Excess 3 converter.
9. Design a Excess 3 to BCD converter.
10. Design a binary to gray code converter.
11. Design a gray code to binary converter.
12. Explain a decoder with an example.
13. Explain a BCD to 7 Segment Decoder with necessary diagrams.
14. Inplement the following function using using 8 : 1 MUX.

    $F(A,B,C,D) = \sum m\ (0,1,3,4,8,9,15)$

    $F(A,B,C,D) = A'BD' + ACD + B'CD + A'C'D$

    $F(A,B,C,D) = \sum m\ (0,2,6,10,11,12,13) + d(3,8,14)$

    $F(A,B,C,D) = \sum m\ (0,1,3,5,8,9,15)$

    $F(A,B,C) = \prod M\ (2,3,4,7)$

15. Design a 4 bit Comparator.

16. Design a 1 : 8 DEMUX using two 1 : 4 DEMUX.

UNIT III

PART A

1. Draw the block diagram of a sequential logic circuit.
2. Differentiate a combinational and sequential logic circuit.
3. Name the two sequential logic circuits.
4. Give the truth table and excitation table for SR flipflop.
5. Give the truth table and excitation table for JK flipflop.
6. Give the truth table and excitation table for D flipflop.
7. Give the truth table and excitation table for T flipflop.
8. Draw the circuit of a master slave JK flipflop.
9. Define Edge Triggering.
10. What is a Counter?
11. Name the different types of counters.
12. Define transition table.
13. Define State table
14. What is UP/DOWN counter?
15. How many no of flipflops are required to design a MOD 9 counter?
16. For the state table given below, draw the state diagram.

Present state	Next state		output
	X = 0	X = 1	
A	A	C	0
B	B	A	0
C	D	C	1
D	B	D	0

17. Draw the block diagram of an asynchronous sequential circuit.

18. What is a primitive flow table?

19. Name the two types of asynchronous sequential circuit.

20. Derive the state equations A(t+1) and B(t+1) for the given input equation of a JK flip

    flop.

$J_A = BX' + B'X$ $K_A = B'X$

$J_B = AX'$ $K_B = A + BX$

21. What is the difference between a state table and a transition table?

22. Define state equation.

23. Draw the block diagram of an asynchronous sequential circuit.

24. What does a ring counter consist of?

PART B

1. Design a MOD 6 counter using T flip flop. Write state table and reduce the expression using K – map.

2. A sequential circuit with two D flip flops A and B , two inputs x and y and one output Z is specified by the following next state and output equations:

$A(t+1) = x'y + xA$

$B(t+1) = x'B + xA$

$Z = B$

Draw the logic diagram and state diagram of the circuit.

3. A sequential circuit with two JK flip flops A and B , two inputs x and y and one output Z is specified by the following next state and output equations:

$J_A = BX + B'Y'$ $K_A = B'XY'$

$J_B = A'X$ $K_B = A + XY'$

$Z = AX'Y' + BX'Y'$

Draw the logic diagram and state diagram.

4. Design a synchronous counter for 4,6,7,3,1,4. using JK flip flop.

5. Design a 4 Bit Binary Ripple Counter using T flip flop.

6. Design a Johnson Counter using D flip flop.

7. Deign a counter with the following repeated binary sequence 0,1,2,4,6.

   Use D flip flop.

8. Design a synchronous counter for 0,1,2,3,4,5,6 using JK flip flop.

9. Design a synchronous counter for 0,1,2,4,6 using D flip flop.

10. A sequential circuit has two JK flipflops A and B and one input X. The circuit is described by the following flipflop input equations:

    $J_A = X$ $K_A = B'$

    $J_B = X$ $K_B = A$

    (a) Derive the state equations A(t+1) and B(t+1) by substituting the input equations

    for the J and K variables.

11. Design a sequential circuit with two D flip flops A and B and one output X. When X = 0, the state of the circuit remains the same. When X = 1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats.

12. Design a sequential circuit with two JK flipflops A and B and two inputs E and X. If E = 0, the circuit remains in the same state regardless of the value of X. When E = 1 and X = 1, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00 and repeats. When E = 0 and X = 0, the circuit goes through the state transitions from 00 to 1 to 10 to 01 back to 00 and repeats.

13. Design a MOD 6 Synchronous counter using JK flipflop.

14. Design a MOD 6 Synchronous counter using T flipflop.

15. Design a MOD Synchronous counter using SR flipflop.

16. Explain the working of 4-bit synchronous counter with the help of timing diagram.

17. Draw and explain the working of 4-bit UP/DOWN counter.

18. How do you construct D flipflop and t flip flop using JK flipflop.

19. Design a sequential circuit with Jk flipflops to satisfy the state equations.

$A(t+1) = A'B'CD + A'B'C + ACD + AC'D'$

$B(t+1) = A'C + CD' + A'BC'$

$C(t+1) = B$ and $D(t+1) = D'$

UNIT IV

PART A

1. What is a primitive flow table?
2. Name the two types of asynchronous sequential circuit.
3. Draw the block diagram of asynchronous sequential logic circuit.
4. Define fundamental mode asynchronous sequential logic circuit.
5. Define pulse mode asynchronous sequential logic circuit.
6. Define stable state.
7. What is race condition? Name its types.
8. Define Critical race.
9. Define Non-Critical race.
10. What is a Cycle?
11. What is meant by state assignment?
12. List the different techniques used for state assignment.
13. Why state reduction is necessary in a sequential circuit?

PART B

1. Design an asynchronous sequential circuit that has two inputs X_1 and X_2 one output Z. When $X_1 = 0$, the output Z is 0. The first change in X_2 occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0.
2. An asynchronous sequential circuit is described by the following excitation and output function.

   $Y = X_1X'_2 + (X_1 + X'_2)\, Y$

$Z = Y$

(a) Draw the logic diagram of the circuit.

(b) Derive the transition table and output map.

3. An asynchronous sequential circuit has two internal states and one output. Excitation and output function describing the circuit are as follows.

$Y_1 = X_1X_2 + X_1Y_2 + X_2Y_1$

$Y_2 = X_2 + X_1Y_1Y_2 + X_1Y_1$

$Z = X_2 + Y_1$

4. Obtain a primitive flow table for a circuit with two inputs and two outputs that satisfies the following conditions.

(i) When inputs $X_1X_2 = 00$, outputs $Z_1Z_2 = 00$,

(ii) When $X_1 = 1$, X_2 changes from 0 to 1, $Z_1Z_2 = 01$,

(iii) When $X_2 = 1$, X_1 changes from 0 to 1, $Z_1Z_2 = 10$,

(iv) Otherwise the output does not change.

5. Design T flipflop from logic gates.

6. Design an asynchronous sequential circuit that has two inputs X_1 and X_2 one output Z. Initially both inputs and output are equal to zero. When X_1 or X_2 become 1, Z becomes 1. When the second input also becomes 1, the output changes to 0. The output stays at 0 until the circuit goes back to the initial state. Obtain a primitive flow table fro the circuit.

7. Explain the steps for the design of asynchronous sequential circuit.

8. Write short notes on Critical and Non-critical races.

9. Explain the two asynchronous sequential circuits.

UNIT V

PART A

1. Define noise margin.
2. What is current sinking and current sourcing action?
3. What is the difference between PAL and PLA?
4. Define V_{IH} (min) and V_{IL} (max) of an IC. What is the value of V_{IH} (min) and V_{IL} (max) of TTL 74 LS series.
5. What is CPLD? Give the floor plan of a typical CPLD?
6. Classify different types of digital memories.
7. List out some of the digital logic families used to construct digital circuits.
8. Define fan in and Fan out.
9. State the principle by which the ECL circuits operate.
10. What are the three types of PLD s available?
11. Draw a block diagram of a memory cell.
12. What does a ROM consists of?
13. Classify different types of ROM.
14. How programming and erasing is done in EPROM?
15. How programming and erasing is done in EEPROM?
16. Draw the block diagram of PLA.
17. Define PLA program table.
18. Define PAL program table.
19. Differentiate PLA, PAL and ROM.
20. Give the classifications of PLDs.

21. What is a PLD?

22. Draw the block diagram of FPGA.

23. What is FPGA?

24. Name the different blocks of CPLD.

25. Draw the circuit of a CMOS NAND gate.

26. Draw the circuit of a CMOS NOR gate.

27. Draw the circuit of a CMOS inverter gate.

PART B

1. With the help of circuit diagram explain the operation of
   - NMOS Inverter
   - CMOS Inverter
   - CMOS NOR Gate
   - CMOS NAND Gate
2. Using ECL basic circuit, explain the operation of
   - ECL Inverter
   - ECL OR/NOR Gate
3. Explain the working of
   - TTL NAND gate
   - TTL NOR gate
4. With the help of block diagram, explain the construction of PLA.
5. A combinational circuit is defined by the function

   $W(A,B,C,D) = \sum m\ (1,2,5,7,8,10,12,14)$

   $X(A,B,C,D) = \sum m\ (0,2,6,8,9,14)$

   $Y(A,B,C,D) = \sum m\ (0,3,7,9,11,12,14)$

   $Z(A,B,C,D) = \sum m\ (1,2,4,5,9,10,14)$

   Implement the circuit with a PLA.
6. Implement the following Boolean expression using ROM

   $F_1 = \Sigma\ (0, 2, 4, 7)$

   $F_2 = \Sigma\ (1, 3, 5, 7)$

10. Explain the various types of ROM.

11. Tabulate the PLA programmable table for the four Boolean functions listed below.

$A(x,y,z) = \sum m\ (0,1,2,4,6)$

$B(x,y,z) = \sum m\ (0,2,6,7)$

$C(x,y,z) = \sum m\ (3,6)$ $D(x,y,z) = \sum m\ (1,3,5,7)$