Karunya UNIVERSITY
Karunya Institute of Technology and Sciences
(Declared under section-3 of the UGC Act, 1956)
KARUNYA NAGAR, COIMBATORE 641 114.

SCHOOL OF ELECTRICAL SCIENCES

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

2012 - 2013

09EE217 – LINEAR AND DIGITAL IC LABORATORY

CREDIT 0:0:2

Course / Branch: B.Tech - EEE

Semester: V

Reg.No	Name of the Student	Faculty Signature

TABLE OF CONTENTS

Expt. No: 1A	A. STUDY OF BASIC DIGITAL ICs
Date:	

OBJECTIVE:

To verify the truth table of basic digital ICs of AND, OR, NOT, NAND, NOR, EX-OR gates.

EQUIPMENTS/COMPONENTS REQUIRED:

S.No	Equipments/Components required	Range	Quantity
1	Digital IC trainer kit	-	1
2	AND gate	IC 7408	1
3	OR gate	IC 7432	1
4	NOT gate	IC 7404	1
5	NAND gate	IC 7400	1
6	NOR gate	IC 7402	1
7	EX-OR gate	IC 7486	1

THEORY:

a. AND gate:

An AND gate is the physical realization of logical multiplication operation. It is an electronic circuit which generates an output signal of '1' only if all the input signals are '1'.

b. OR gate:

An OR gate is the physical realization of the logical addition operation. It is an electronic circuit which generates an output signal of '1' if any of the input signal is '1'.

c. NOT gate:

A NOT gate is the physical realization of the complementation operation. It is an electronic circuit which generates an output signal which is the reverse of the input signal. A NOT gate is also known as an inverter because it inverts the input.

d. NAND gate:

A NAND gate is a complemented AND gate. The output of the NAND gate will be '0' if all the input signals are '1' and will be '1' if any one of the input signal is '0'.

e. NOR gate:

A NOR gate is a complemented OR gate. The output of the OR gate will be '1' if all the inputs are '0' and will be '0' if any one of the input signal is '1'.

f. EX-OR gate:

An Ex-OR gate performs the following Boolean function,

$$A \oplus B = (A . B') + (A' . B)$$

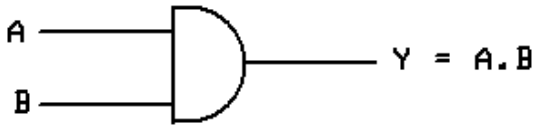
It is similar to OR gate but excludes the combination of both A and B being equal to one. The exclusive OR is a function that give an output signal '0' when the two input signals are equal either '0' or '1'.

PROCEDURE:

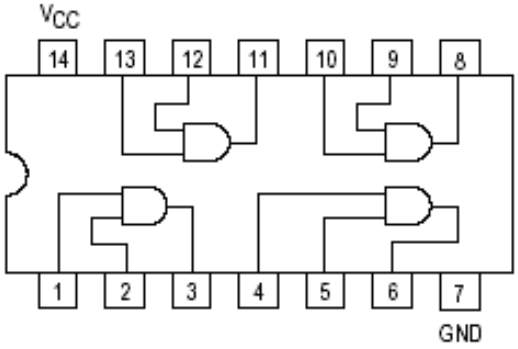
1. Connections are given as per the circuit diagram
2. For all the ICs 7th pin is grounded and 14th pin is given +5 V supply.
3. Apply the inputs and verify the truth table for all gates.

AND GATE

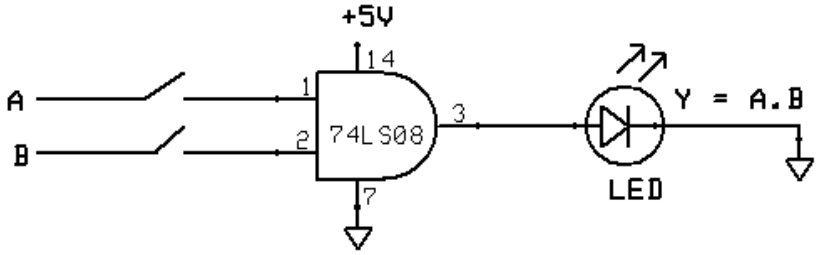
LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7408 :



CIRCUIT DIAGRAM:



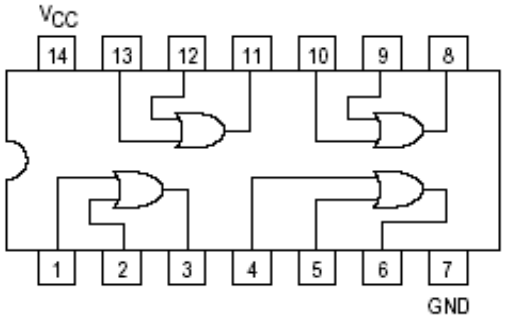
TRUTH TABLE:

S.No	INPUT		OUTPUT
	A	B	Y = A . B
1.	0	0	0
2.	0	1	0
3.	1	0	0
4.	1	1	1

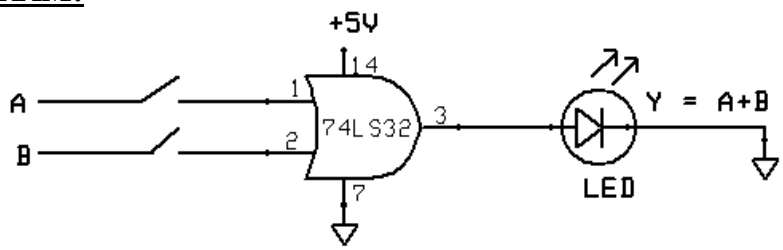
OR GATE

LOGIC DIAGRAM:

PIN DIAGRAM OF IC 7432:



CIRCUIT DIAGRAM:

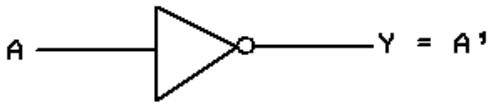


TRUTH TABLE:

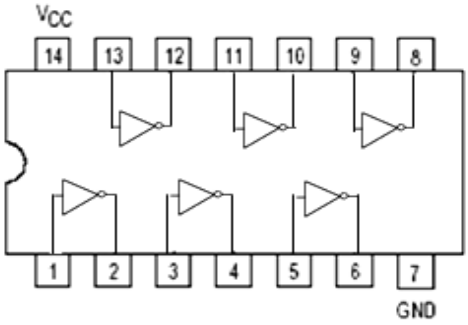
S.No	INPUT		OUTPUT
	A	B	Y = A + B
1.	0	0	0
2.	0	1	1
3.	1	0	1
4.	1	1	1

NOT GATE

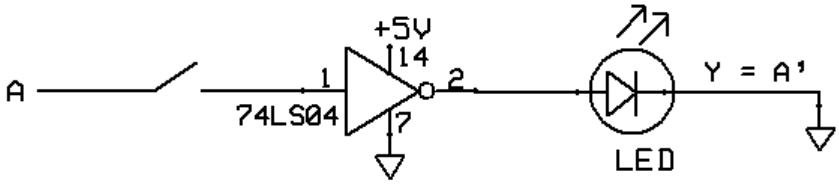
LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7404:



CIRCUIT DIAGRAM:

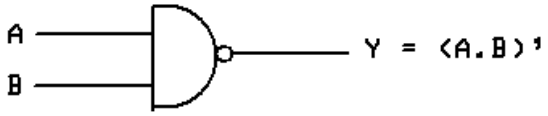


TRUTH TABLE:

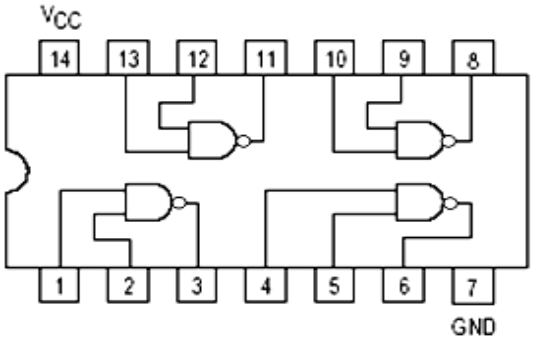
S.No	INPUT	OUTPUT
	A	Y = A'
1.	0	1
2.	1	0

NAND GATE

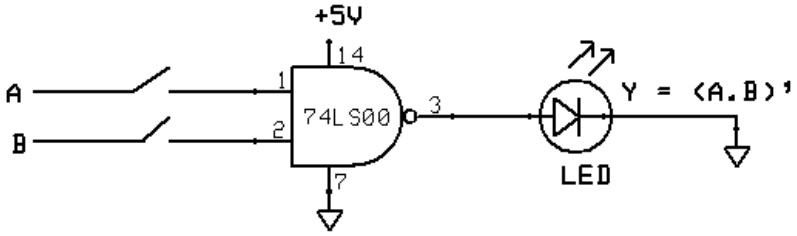
LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7400:



CIRCUIT DIARAM:

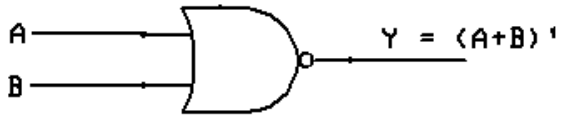


TRUTH TABLE:

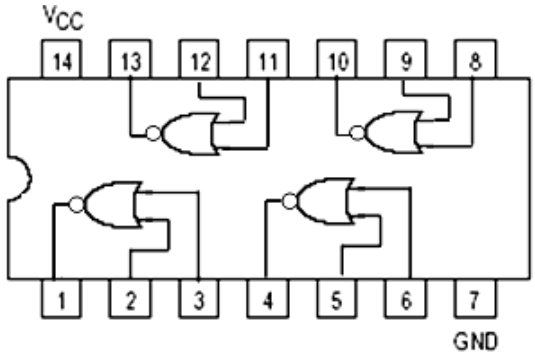
S.No	INPUT		OUTPUT
	A	B	Y = (A. B)'
1.	0	0	1
2.	0	1	1
3.	1	0	1
4.	1	1	0

NOR GATE

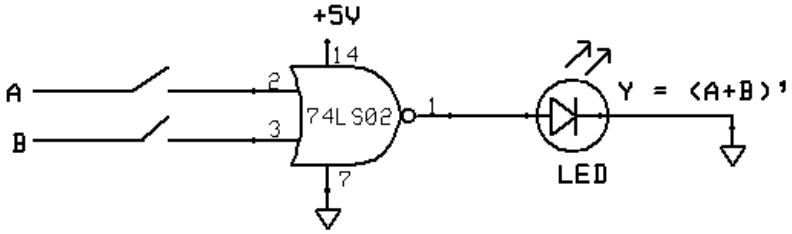
LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7402:



CIRCUIT DIAGRAM:

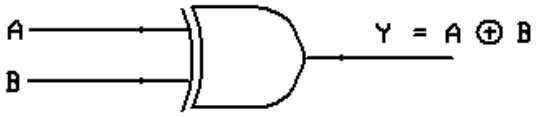


TRUTH TABLE:

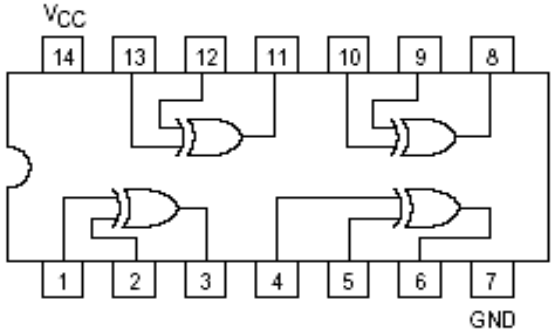
S.No	INPUT		OUTPUT
	A	B	Y = (A + B)'
1.	0	0	1
2.	0	1	0
3.	1	0	0
4.	1	1	0

EX-OR GATE

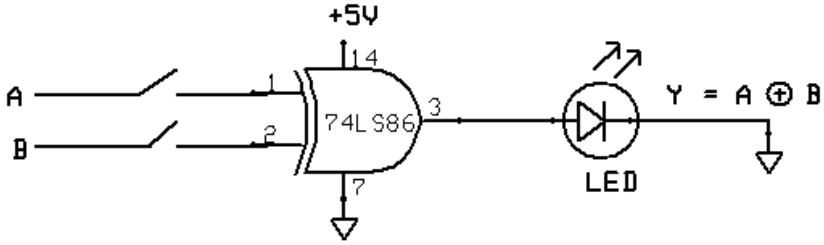
LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7486:



CIRCUIT DIAGRAM:



TRUTH TABLE:

S.No	INPUT		OUTPUT
	A	B	Y = A ⊕ B
1.	0	0	0
2.	0	1	1
3.	1	0	1
4.	1	1	0

RESULT:

The truth table of all the basic digital ICs were verified.

VIVA QUESTIONS:

1. What is a Logic gate?
2. Give the classification of logic families
3. What are the basic digital logic gates?
4. Which gates are called as the universal gates? What are its advantages?
5. Classify the logic family by operation?

Expt. No: 1 B	B. STUDY OF FLIP FLOPS
Date:	

OBJECTIVE:

To verify the characteristic table of RS, D, JK, and T Flip flops.

EQUIPMENTS/COMPONENTS REQUIRED:

S.No	Equipments/Components required	Range	Quantity
1	Digital IC trainer kit	-	1
2	NOR gate	IC 7402	1
3	NOT gate	IC 7404	1
4	AND gate (three input)	IC 7411	1
5	NAND gate	IC 7400	1

THEORY:

A Flip Flop is a sequential device that samples its input signals and changes its output states only at times determined by clocking signal. Flip Flops may vary in the number of inputs they possess and the manner in which the inputs affect the binary states.

RS FLIP FLOP:

The clocked RS flip flop consists of NAND gates and the output changes its state with respect to the input on application of clock pulse. When the clock pulse is high the S and R inputs reach the second level NAND gates in their complementary form. The Flip Flop is reset when the R input high and S input is low. The Flip Flop is set when the S input is high and R input is low. When both the inputs are high the output is in an indeterminate state.

D FLIP FLOP:

To eliminate the undesirable condition of indeterminate state in the SR Flip Flop when both inputs are high at the same time, in the D Flip Flop the inputs are never made equal at the same time. This is obtained by making the two inputs complement of each other.

JK FLIP FLOP:

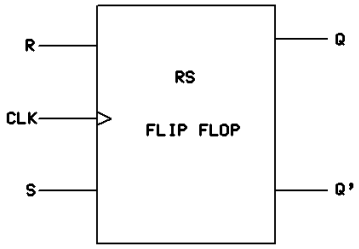
The indeterminate state in the SR Flip-Flop is defined in the JK Flip Flop. JK inputs behave like S and R inputs to set and reset the Flip Flop. The output Q is ANDed with K input and the clock pulse, similarly the output Q' is ANDed with J input and the Clock pulse. When the clock pulse is zero both the AND gates are disabled and the Q and Q' output retain their previous values. When the clock pulse is high, the J and K inputs reach the NOR gates. When both the inputs are high the output toggles continuously. This is called Race around condition and this must be avoided.

T FLIP FLOP:

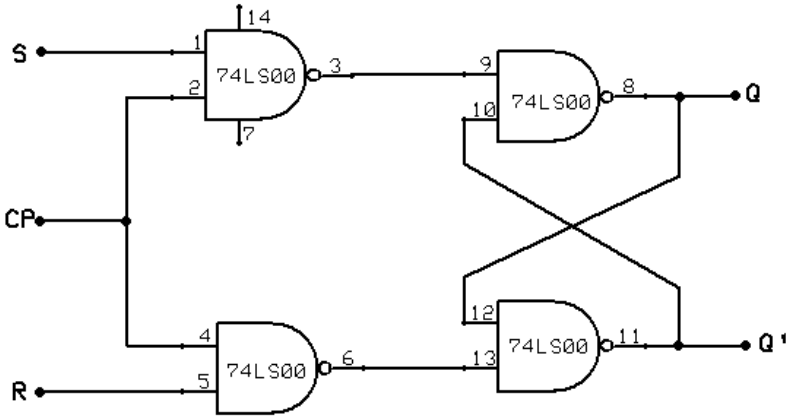
This is a modification of JK Flip Flop, obtained by connecting both inputs J and K inputs together. T Flip Flop is also called Toggle Flip Flop.

RS FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:

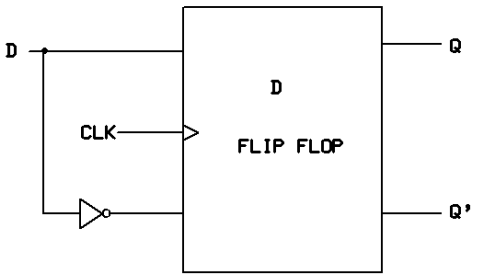


CHARACTERISTIC TABLE:

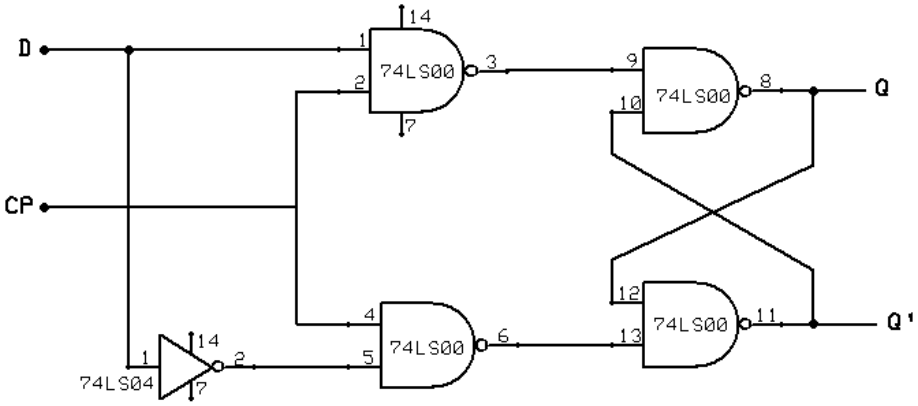
CLOCK PULSE	INPUT		PRESENT STATE (Q_n)	NEXT STATE(Q_{n+1})	STATUS
	S	R			
1	0	0	0	0	
2	0	0	1	1	
3	0	1	0	0	
4	0	1	1	0	
5	1	0	0	1	
6	1	0	1	1	
7	1	1	0	X	
8	1	1	1	X	

D FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:

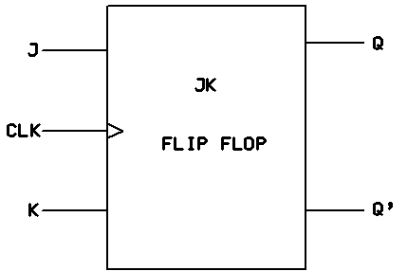


CHARACTERISTIC TABLE:

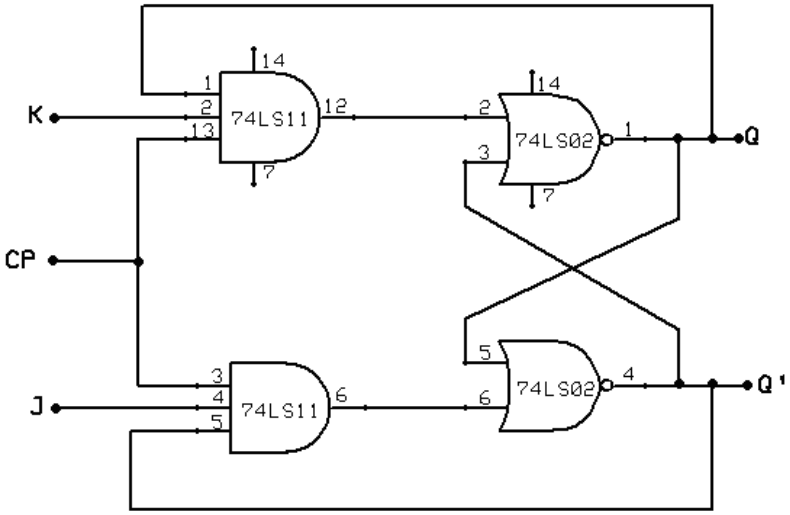
CLOCK PULSE	INPUT D	PRESENT STATE (Q_n)	NEXT STATE(Q_{n+1})	STATUS
1	0	0	0	
2	0	1	0	
3	1	0	1	
4	1	1	1	

JK FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:

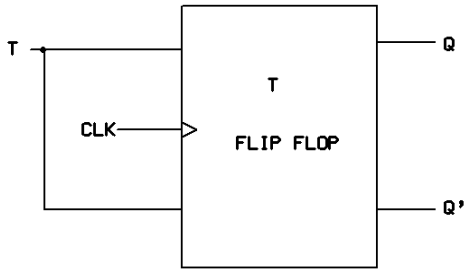


CHARACTERISTIC TABLE:

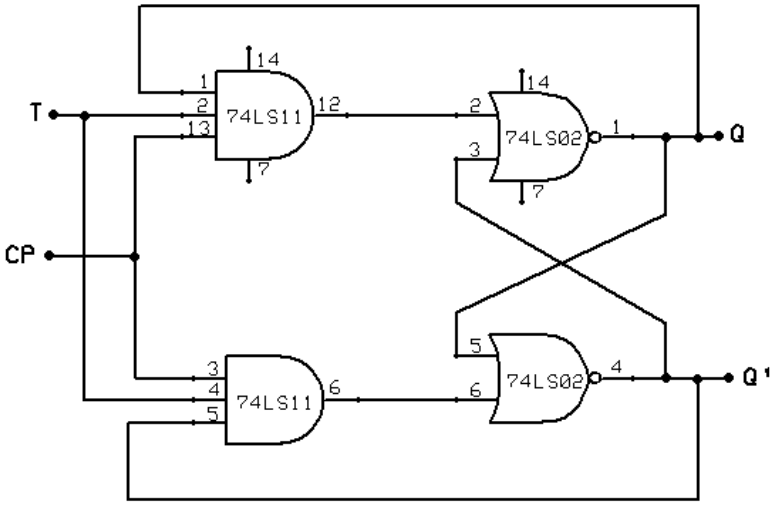
CLOCK PULSE	INPUT		PRESENT STATE (Q_n)	NEXT STATE(Q_{n+1})	STATUS
	J	K			
1	0	0	0	0	
2	0	0	1	1	
3	0	1	0	0	
4	0	1	1	0	
5	1	0	0	1	
6	1	0	1	1	
7	1	1	0	1	
8	1	1	1	0	

T FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:



CHARACTERISTIC TABLE:

CLOCK PULSE	INPUT T	PRESENT STATE (Q_n)	NEXT STATE(Q_{n+1})	STATUS
1	0	0	0	
2	0	1	0	
3	1	0	1	
4	1	1	0	

PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7^{th} pin is grounded and 14^{th} pin is given +5 V supply.
3. Apply the inputs and observe the status of all the flip flops.

RESULT:

The Characteristic tables of RS, D, JK, T flip flops were verified.

VIVA QUESTIONS:

1. Define Flip flop.
2. What are the different types of flip-flop?
3. What is the operation of RS flip-flop?
4. What is the operation of SR flip-flop?
5. What is the operation of D flip-flop?
6. What is the operation of JK flip-flop?
7. What is the operation of T flip-flop?
8. Define race around condition.
9. What is edge-triggered flip-flop?

Expt. No: 2	REALIZATION OF SWITCHING FUNCTIONS USING NAND OR NOR GATE
Date:	

OBJECTIVE:

To realize the following switching function using NAND or NOR gate and verify the truth table.

F (A, B, C, D) = Σ (0, 1, 2, 5, 8, 9, 10)

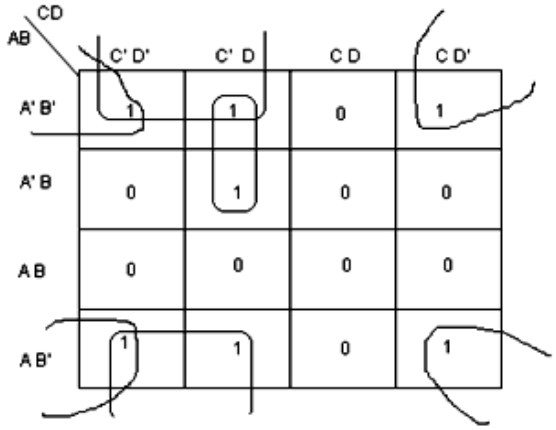
EQUIPMENTS/COMPONENTS REQUIRED:

S.No	Equipments/Components required	Range	Quantity
1	Digital IC trainer kit	-	1
2	NAND gate	IC 7400	As required
3	NOT gate	IC 7404	As required

DESIGN:

Given , F (A,B,C,D) = Σ (0, 1, 2, 5, 8, 9, 10)

The output function F has four input variables hence a four variable Karnaugh Map is used to obtain a simplified expression for the output as shown,



From the K-Map,

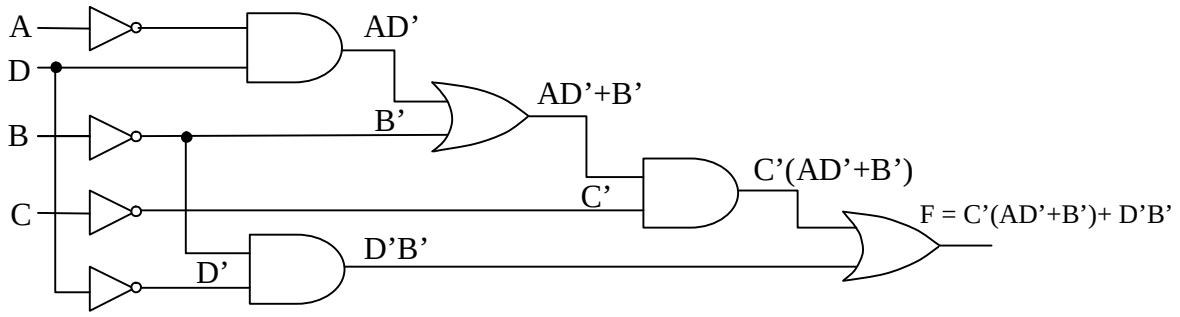
F = B’ C’ + D’ B’ + A’ C’ D

Since we are using only two input logic gates the above expression can be re-written as,

F = C’ (B’ + A’ D) + D’ B’

Now the logic circuit for the above equation can be drawn.

CIRCUIT DIAGRAM:



Convert the above logic diagram to NAND or NOR logic using the following procedure and verify the following truth table.

NAND logic conversion:

Step 1: Draw the AND/OR logic diagram.
Step 2: Add bubbles on output of each AND gate and bubbles on input side to all OR gates.
Step 3: Add or subtract an inverter on each line that received a bubble in step 2.
Step 4: Replace bubbled OR by NAND gate.

NOR logic conversion:

Step 1: Draw the AND/OR logic diagram.
Step 2: Add bubbles on output of each OR gate and bubbles on input side to all AND gates.
Step 3: Add or subtract an inverter on each line that received a bubble in step 2.
Step 4: Replace bubbled AND by NOR gate.

TRUTH TABLE:

S.No	INPUT				OUTPUT
	A	B	C	D	F=D'B'+C'(B'+A'D)
1.	0	0	0	0	1
2.	0	0	0	1	1
3.	0	0	1	0	1
4.	0	0	1	1	0
5.	0	1	0	0	0
6.	0	1	0	1	1
7.	0	1	1	0	0
8.	0	1	1	1	0
9.	1	0	0	0	1
10.	1	0	0	1	1
11.	1	0	1	0	1
12.	1	0	1	1	0
13.	1	1	0	0	0
14.	1	1	0	1	0
15.	1	1	1	0	0
16.	1	1	1	1	0

PROCEDURE:

1. Connections are given as per the circuit diagram
2. For all the ICs 7^{th} pin is grounded and 14^{th} pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the given Boolean expression.

RESULT:

The truth table of the given Boolean expression was verified.

VIVA QUESTIONS:

1. Which gate is equal to AND-invert Gate?
2. Which gate is equal to OR-invert Gate?
3. Bubbled OR gate is equal to----------
4. Bubbled AND gate is equal to----------

Expt. No: 3 A	A. IMPLEMENTATION OF HALF ADDER & FULL ADDER
Date:	

OBJECTIVE:

To design and verify the truth table of the Half Adder & Full Adder circuits.

EQUIPMENTS/COMPONENTS REQUIRED:

S.No	Equipments/Components required	Range	Quantity
1	Digital IC trainer kit	-	1
2	AND gate	IC 7408	1
3	OR gate	IC 7432	1
4	NOT gate	IC 7404	1
5	EX-OR gate	IC 7486	1

THEORY:

The most basic arithmetic operation is the addition of two binary digits. There are four possible elementary operations, namely,

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 10_2$$

The first three operations produce a sum of whose length is one digit, but when the last operation is performed the sum is two digits. The higher significant bit of this result is called a carry and lower significant bit is called the sum.

HALF ADDER:

A combinational circuit which performs the addition of two bits is called half adder. The input variables designate the augend and the addend bit, whereas the output variables produce the sum and carry bits.

FULL ADDER:

A combinational circuit which performs the arithmetic sum of three input bits is called full adder. The three input bits include two significant bits and a previous carry bit. A full adder circuit can be implemented with two half adders and one OR gate.

HALF ADDER

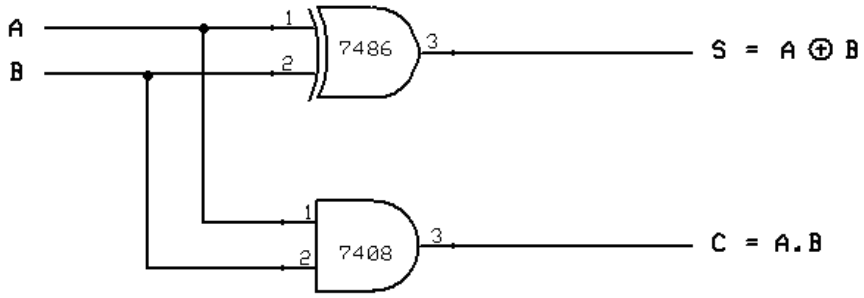
TRUTH TABLE:

S.No	INPUT		OUTPUT	
	A	B	S	C
1.	0	0	0	0
2.	0	1	1	0
3.	1	0	1	0
4.	1	1	0	1

DESIGN:

From the truth table the expression for sum and carry bits of the output can be obtained as,
Sum, S = A $\oplus$ B
Carry, C = A . B

CIRCUIT DIAGRAM:



FULL ADDER

TRUTH TABLE:

S.No	INPUT			OUTPUT	
	A	B	C	SUM	CARRY
1.	0	0	0	0	0
2.	0	0	1	1	0
3.	0	1	0	1	0
4.	0	1	1	0	1
5.	1	0	0	1	0
6.	1	0	1	0	1
7.	1	1	0	0	1
8.	1	1	1	1	1

DESIGN:

From the truth table the expression for sum and carry bits of the output can be obtained as,

SUM = A'B'C + A'BC' + AB'C' + ABC
CARRY = A'BC + AB'C + ABC' +ABC
Using Karnaugh maps the reduced expression for the output bits can be obtained as,

SUM

A \ BC	B'C'	B'C	BC	BC'
A'	0	(1)	0	(1)
A	(1)	0	(1)	0

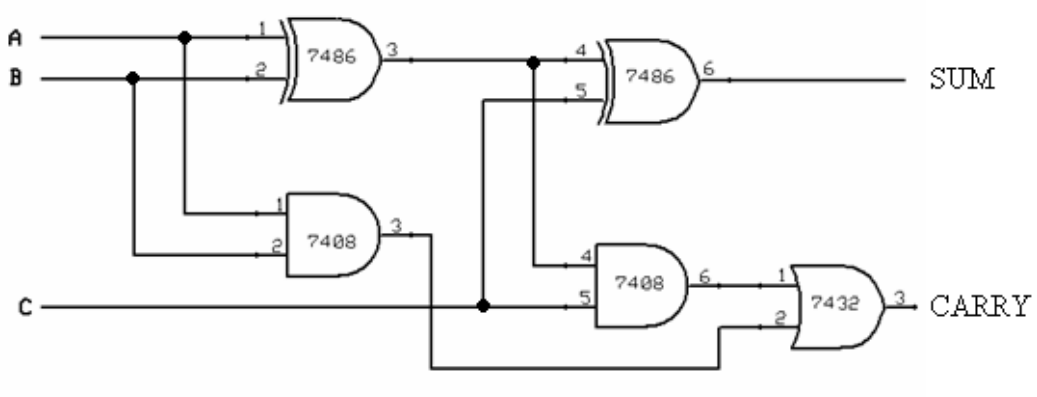
SUM = A'B'C + A'BC' + AB'C' + ABC = A ⊕ B ⊕ C

CARRY

A \ BC	B'C'	B'C	BC	BC'
A'	0	0	1	0
A	0	1	1	1

CARRY = AB + AC + BC

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7^{th} pin is grounded and 14^{th} pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the half adder and full adder circuits.

RESULT:

The design of the half adder and full adder circuits was done and their truth tables were verified.

VIVA QUESTIONS:

1. Define combinational logic
2. Explain the design procedure for combinational circuits
3. Define Half adder and full adder

Expt. No: 3 B	B. IMPLEMENTATION OF HALF SUBTRACTOR & FULL SUBTRACTOR
Date:	

OBJECTIVE:

To design and verify the truth table of the Half Subtractor & Full Subtractor circuits.

EQUIPMENTS/COMPONENTS REQUIRED:

S.No	Equipments/Components required	Range	Quantity
1	Digital IC trainer kit	-	1
2	AND gate	IC 7408	1
3	OR gate	IC 7432	1
4	NOT gate	IC 7404	1
5	EX-OR gate	IC 7486	1

THEORY:

The arithmetic operation, subtraction of two binary digits has four possible elementary operations, namely,

0 - 0 = 0
0 - 1 = 1 with 1 borrow
1 - 0 = 1
1 - 1 = 0

In all operations, each subtrahend bit is subtracted from the minuend bit. In case of the second operation the minuend bit is smaller than the subtrahend bit, hence 1 is borrowed.

HALF SUBTRACTOR:

A combinational circuit which performs the subtraction of two bits is called half subtractor. The input variables designate the minuend and the subtrahend bit, whereas the output variables produce the difference and borrow bits.

FULL SUBTRACTOR:

A combinational circuit which performs the subtraction of three input bits is called full subtractor. The three input bits include two significant bits and a previous borrow bit. A full subtractor circuit can be implemented with two half subtractors and one OR gate.

HALF SUBTRACTOR

TRUTH TABLE:

S.No	INPUT		OUTPUT	
	A	B	DIFF	BORR
1.	0	0	0	0
2.	0	1	1	1
3.	1	0	1	0
4.	1	1	0	0

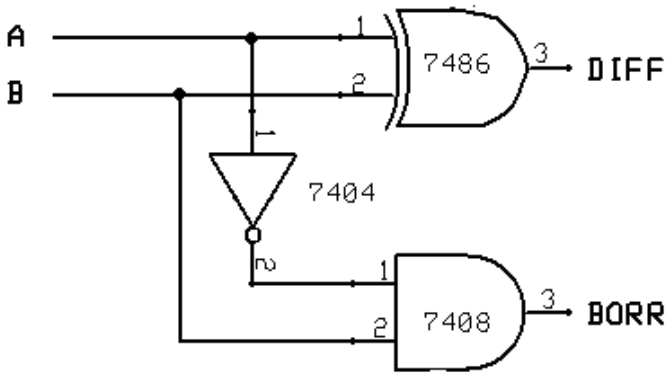
DESIGN:

From the truth table the expression for difference and borrow bits of the output can be obtained as,

Difference, DIFF = A $\oplus$ B

Borrow, BORR = A' . B

CIRCUIT DIAGRAM:



FULL SUBTRACTOR

TRUTH TABLE:

S.No	INPUT			OUTPUT	
	A	B	C	DIFF	BORR
1.	0	0	0	0	0
2.	0	0	1	1	1
3.	0	1	0	1	1
4.	0	1	1	0	1
5.	1	0	0	1	0
6.	1	0	1	0	0
7.	1	1	0	0	0
8.	1	1	1	1	1

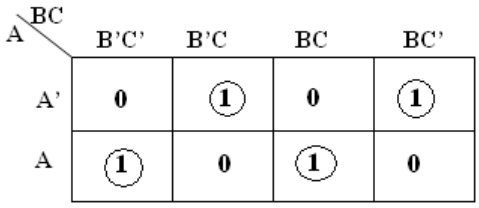
DESIGN:

From the truth table the expression for difference and borrow bits of the output can be obtained as,

Difference, DIFF= A'B'C + A'BC' + AB'C' + ABC
Borrow, BORR = A'BC + AB'C + ABC' +ABC

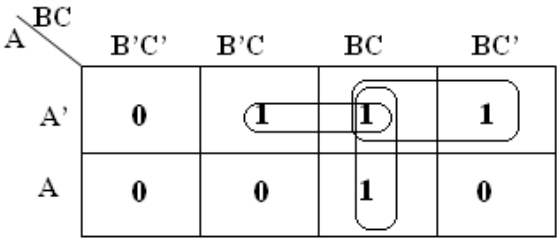
Using Karnaugh maps the reduced expression for the output bits can be obtained as,

DIFFERENCE



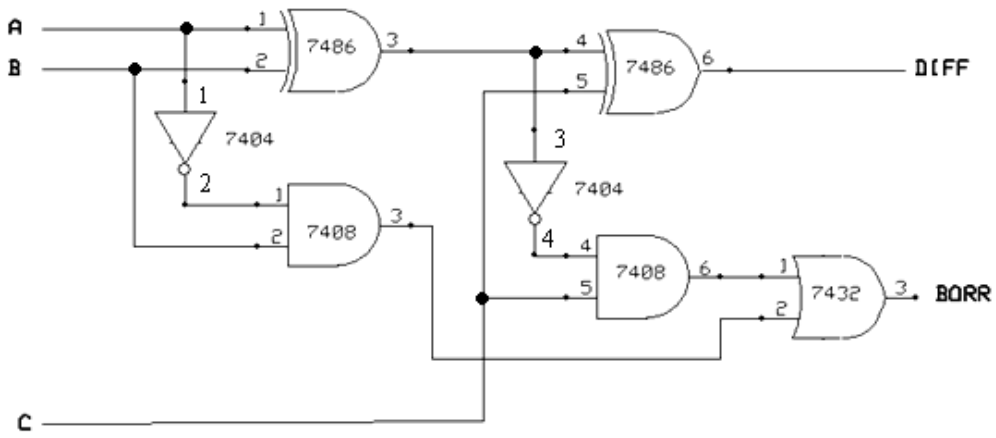
DIFF = A'B'C + A'BC' + AB'C' + ABC = A ⊕ B ⊕ C

BORROW



BORR = A'B + A'C + BC

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7th pin is grounded and 14th pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the half subtractor and full subtractor circuits.

RESULT:

The design of the half subtractor and full subtractor circuits was done and their truth tables were verified.

VIVA QUESTIONS:

1. Define combinational logic
2. What is Full and Half subtractor?
3. What do you mean by comparator?

Expt. No: 4	MULTIPLEXER & DEMULTIPLEXER
Date:	

OBJECTIVE:

To design and verify the truth table of a 4X1 Multiplexer & 1X4 Demultiplexer.

EQUIPMENTS/COMPONENTS REQUIRED:

S.No	Equipments/Components required	Range	Quantity
1	Digital IC trainer kit	-	1
2	AND gate	IC 7408	1
3	OR gate	IC 7432	1
4	NOT gate	IC 7404	1

THEORY:

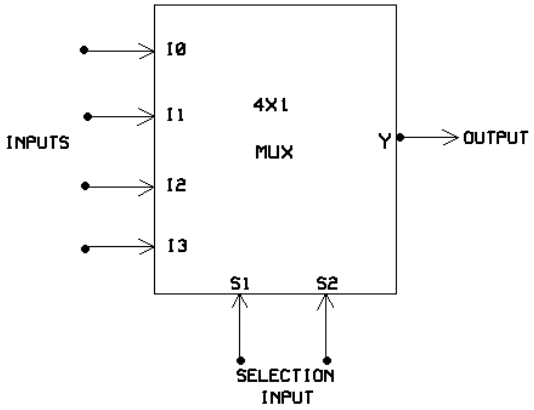
Multiplexer is a digital switch which allows digital information from several sources to be routed onto a single output line. The basic multiplexer has several data input lines and a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^n input lines and n selector lines whose bit combinations determine which input is selected. Therefore, multiplexer is 'many into one' and it provides the digital equivalent of an analog selector switch.

A Demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines. The selection of specific output line is controlled by the values of n selection lines.

DESIGN:

4 X 1 MULTIPLEXER

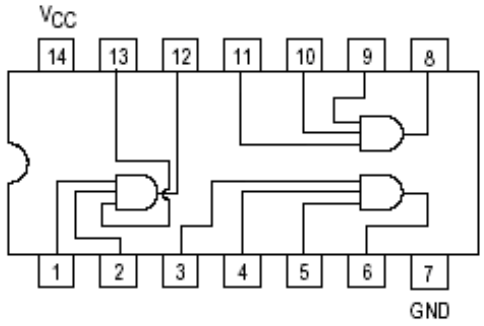
LOGIC SYMBOL:



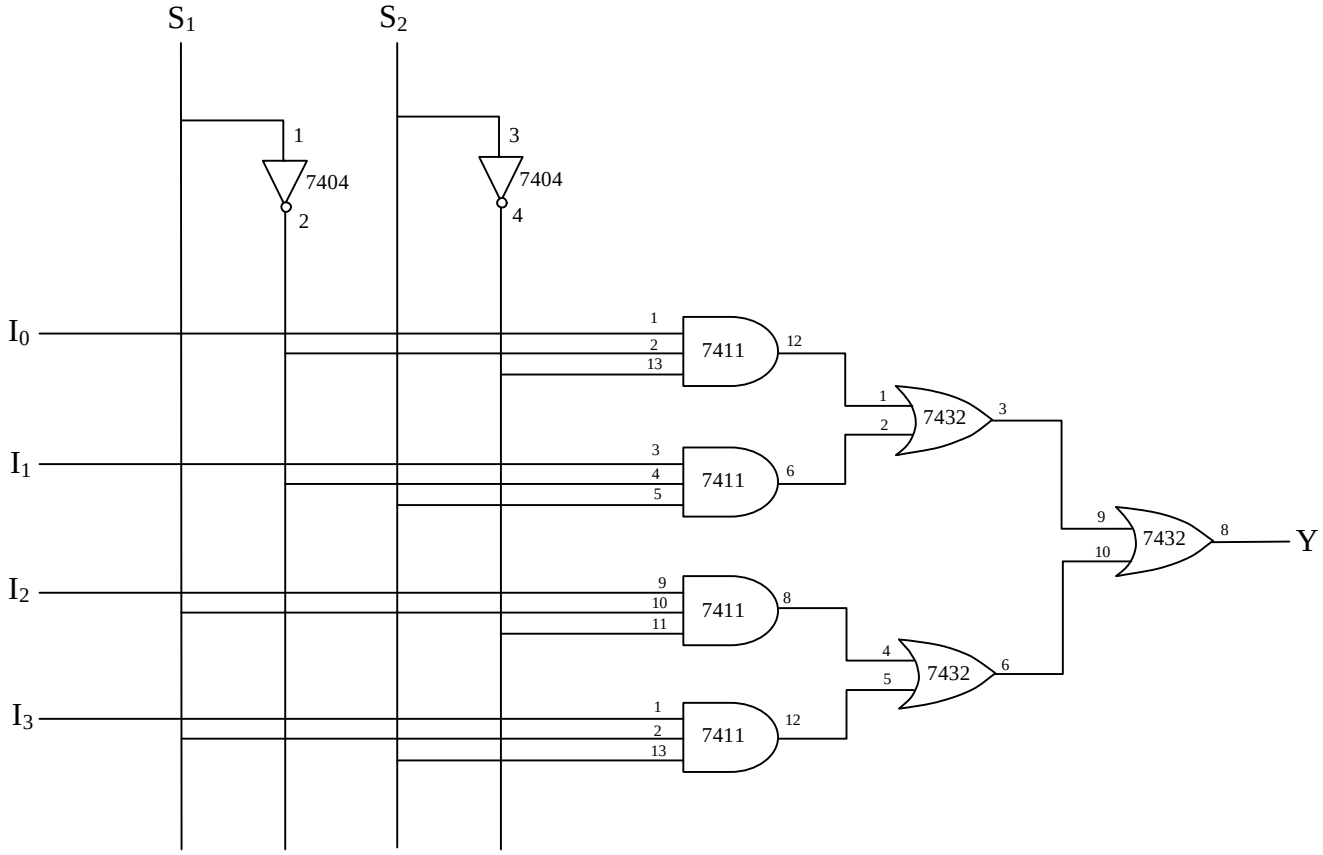
TRUTH TABLE:

S.No	SELECTION INPUT		OUTPUT
	S1	S2	Y
1.	0	0	I_0
2.	0	1	I_1
3.	1	0	I_2
4.	1	1	I_3

PIN DIAGRAM OF IC 7411:

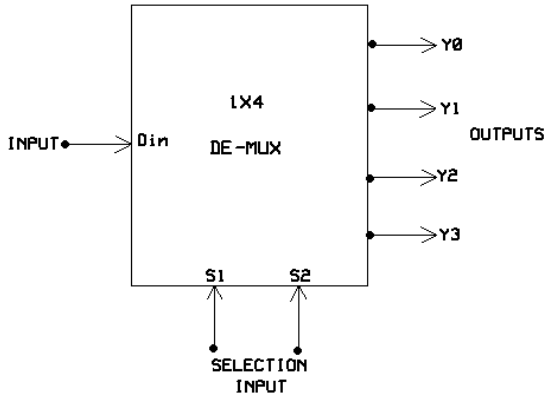


CIRCUIT DIAGRAM:



1X4 DEMULTIPLEXER

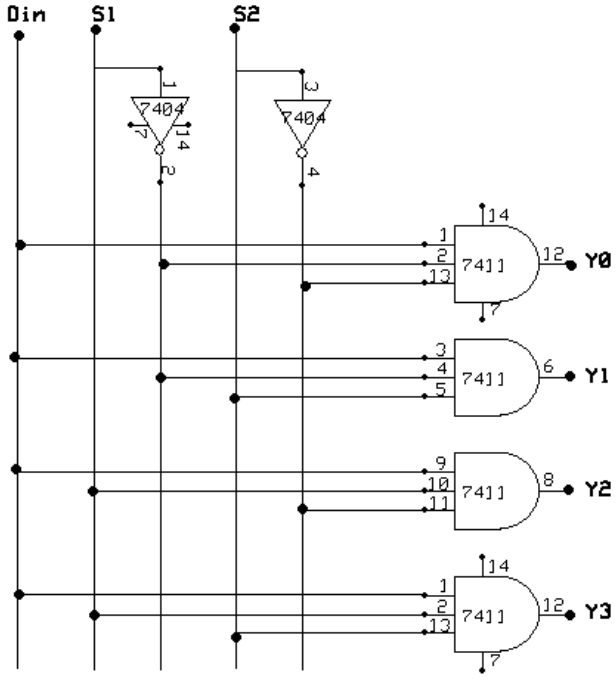
LOGIC SYMBOL:



TRUTH TABLE:

S.No	INPUT			OUTPUT			
	S1	S2	Din	Y0	Y1	Y2	Y3
1.	0	0	0	0	0	0	0
2.	0	0	1	1	0	0	0
3.	0	1	0	0	0	0	0
4.	0	1	1	0	1	0	0
5.	1	0	0	0	0	0	0
6.	1	0	1	0	0	1	0
7.	1	1	0	0	0	0	0
8.	1	1	1	0	0	0	1

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7^{th} pin is grounded and 14^{th} pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the multiplexer & demultiplexer.

RESULT:

The design of the 4x1 Multiplexer and 1x4 Demultiplexer circuits was done and their truth tables were verified.

VIVA QUESTIONS:

1. Define multiplexer.
2. Differentiate Decoder and De multiplexer.

Expt. No: 5	SHIFT REGISTER
Date:	

OBJECTIVE:

To implement and verify the truth table of a serial in serial out shift register.

EQUIPMENTS/COMPONENTS REQUIRED:

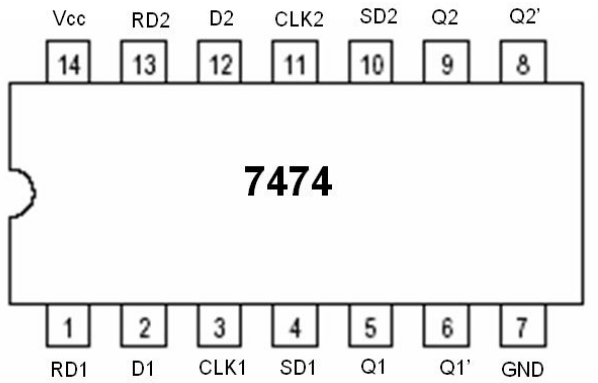
S.No	Equipments/Components required	Range	Quantity
1	Digital IC trainer kit	-	1
2	D Flip Flop	IC 7474	2

THEORY:

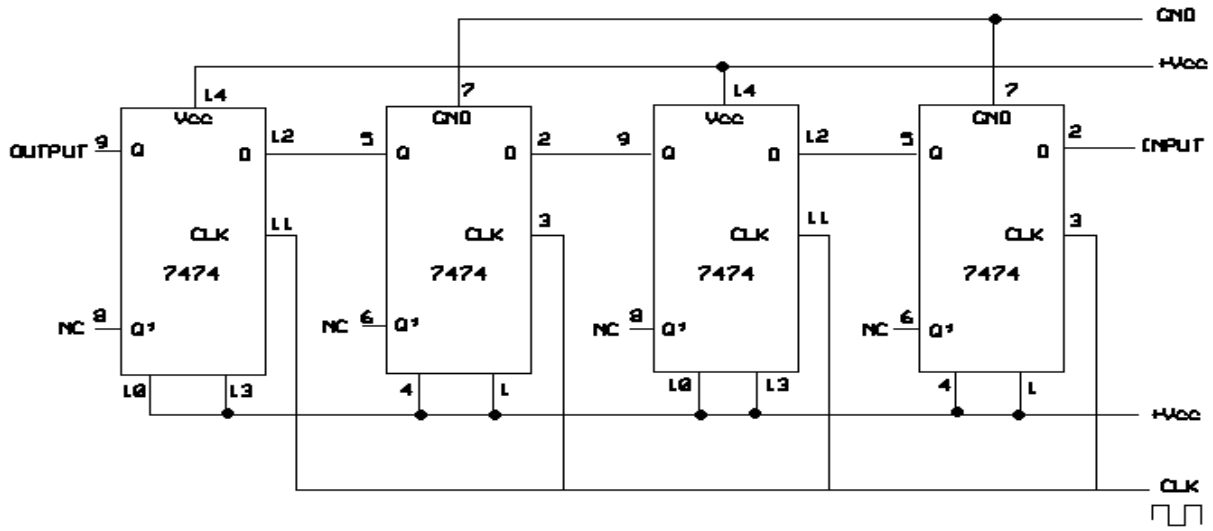
A register capable of shifting its binary information either to the left or to the right is called a shift register. The logical configuration of a shift register consists of a chain of flip flops connected in cascade with the output of one flip flop connected to the input of the next flip flop. All the flip flops receive a common clock pulse which causes the shift from one stage to the next.

The Q output of a D flip flop is connected to the D input of the flip flop to the left. Each clock pulse shifts the contents of the register one bit position to the right. The serial input determines, what goes into the right most flip flop during the shift. The serial output is taken from the output of the left most flip flop prior to the application of a pulse. Although this register shifts its contents to its left, if we turn the page upside down we find that the register shifts its contents to the right. Thus a unidirectional shift register can function either as a shift right or a shift left register.

PIN DIAGRAM OF IC 7474:



CIRCUIT DIAGRAM:



TRUTH TABLE:

For a serial data input of 1101,

S.NO	CLOCK PULSE	INPUTS				OUTPUTS			
		D1	D2	D3	D4	Q1	Q2	Q3	Q4
1	1	1	X	X	X	1	X	X	X
2	2	1	1	X	X	1	1	X	X
3	3	0	1	1	X	0	1	1	X
4	4	1	0	1	1	1	0	1	1
5	5	X	1	0	1	X	1	0	1
6	6	X	X	1	0	1	X	1	0
7	7	X	X	X	1	0	X	X	1
8	8	X	X	X	X	X	X	X	X

PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. Apply the input and verify the truth table of the counter.

RESULT:

The truth table of a serial in serial out left shift register was hence verified.

VIVA QUESTIONS:

1. Define rise and fall time.
2. Define skew and clock skew.
3. Define setup and hold time.
4. Define propagation delay.
5. Define shift registers.
6. What are the different types of shift type?

Expt. No: 6	ASYNCHRONOUS DECADE COUNTER
Date:	

OBJECTIVE:

To implement and verify the truth table of an asynchronous decade counter.

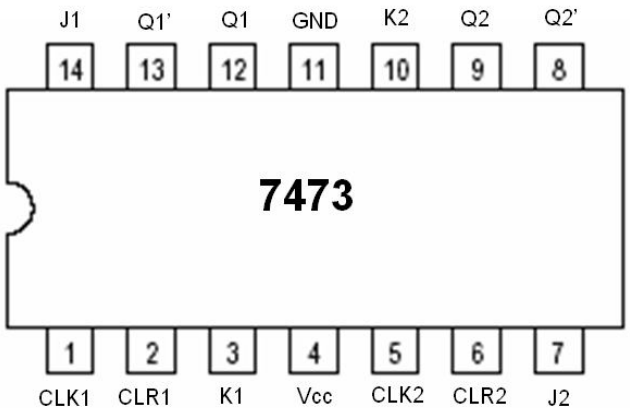
EQUIPMENTS/COMPONENTS REQUIRED:

S.No	Equipments/Components required	Range	Quantity
1	Digital IC trainer kit	-	1
2	JK Flip Flop	IC 7473	2
3	NAND gate	IC 7400	1

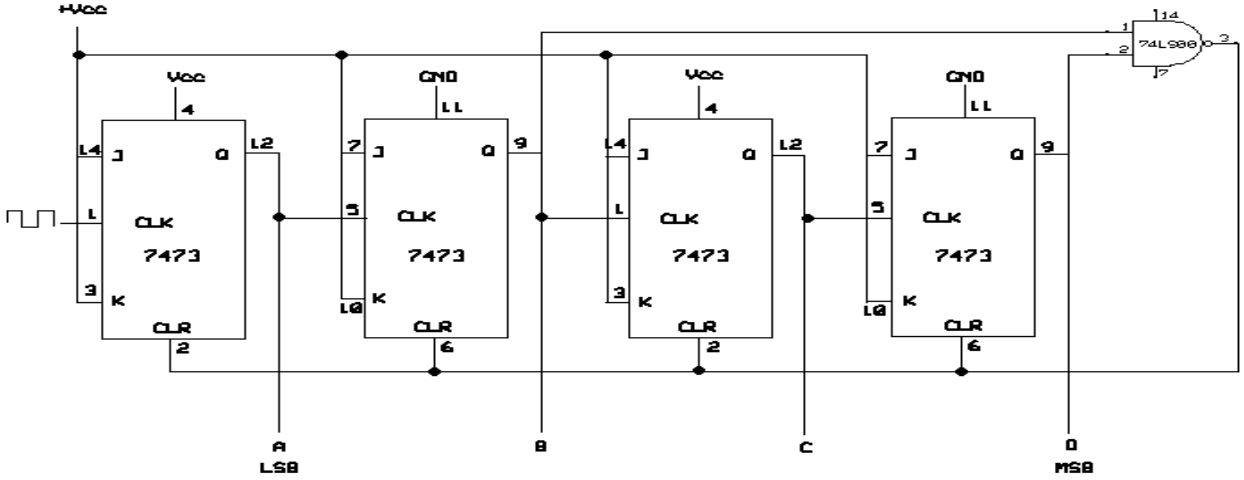
THEORY:

Asynchronous decade counter is also called as ripple counter. In a ripple counter the flip flop output transition serves as a source for triggering other flip flops. In other words the clock pulse inputs of all the flip flops are triggered not by the incoming pulses but rather by the transition that occurs in other flip flops. The term asynchronous refers to the events that do not occur at the same time. With respect to the counter operation, asynchronous means that the flip flop within the counter are not made to change states at exactly the same time, they do not because the clock pulses are not connected directly to the clock input of each flip flop in the counter.

PIN DIAGRAM OF IC 7473:



CIRCUIT DIAGRAM:



TRUTH TABLE:

S.No	CLOCK PULSE	OUTPUT			
		D(MSB)	C	B	A(LSB)
1	-	0	0	0	0
2	1	0	0	0	1
3	2	0	0	1	0
4	3	0	0	1	1
5	4	0	1	0	0
6	5	0	1	0	1
7	6	0	1	1	0
8	7	0	1	1	1
9	8	1	0	0	0
10	9	1	0	1	0
11	10	0	0	0	0

PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. Apply the input and verify the truth table of the counter.

RESULT:

The truth table of the Asynchronous decade counter was hence verified.

VIVA QUESTIONS:

1. Define sequential circuit?
2. Give the comparison between combinational circuits and sequential circuits.
3. What do you mean by present state?
4. What do you mean by next state?
5. State the types of sequential circuits?
6. Give the comparison between synchronous & Asynchronous sequential circuits?

Expt. No: 7	INVERTING & NON-INVERTING AMPLIFIER
Date:	

OBJECTIVE:

To design an inverting amplifier and a non-inverting amplifier and to determine the frequency response of it.

EQUIPMENTS/COMPONENTS REQUIRED:

S.No	Equipments/Components required	Range	Quantity
1	Operational Amplifier IC	µA 741	1
2	Resistors	500 Ω	1
		1 KΩ	2
		2 KΩ	1
		500 Ω	1
		666 Ω	1
4	Regulated Dual power supply	(0 – 30) V	1
5	Function Generator	(0 – 3) MHz	1
6	Cathode ray Oscilloscope	(0 – 30) MHz	1

THEORY:

The operational amplifier is basically a differential amplifier having a large voltage gain and very high input impedance. It has inverting input and non-inverting input and single output. It is powered by dual polarity power supply.

INVERTING AMPLIFIER:

The input signal (V_i) is applied to the inverting input terminal through R_i and the non-inverting input terminal is grounded. The output voltage V_o is fed back to the inverting input terminal through R_f – R_1 network. The gain of an inverting amplifier is given by

$$A = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

DESIGN:

Assume gain A = 2 and R_1 = 1 KΩ

So, $R_f = 2R_1 = 2$ KΩ and

$$R_{comp} = R_f \parallel R_1 = \frac{R_f \times R_f}{R_f + R_1} = \frac{2 \times 1}{2 + 1} = 0.666K\Omega = 666\Omega$$

NON-INVERTING AMPLIFIER:

The input signal is applied to the non-inverting input terminal and the output voltage is fed back to the inverting input terminal. The voltage gain of the non-inverting amplifier is given by

$$A = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$$

DESIGN:

Assume gain A = 2 and R_1 = 1 KΩ

So, $R_f = (2-1)R_1$ = 1 KΩ and

$$R_{comp} = R_f \,||\, R_1 = \frac{R_f \times R_f}{R_f + R_1} = \frac{1 \times 1}{1+1} = 0.500K\Omega = 500\Omega$$

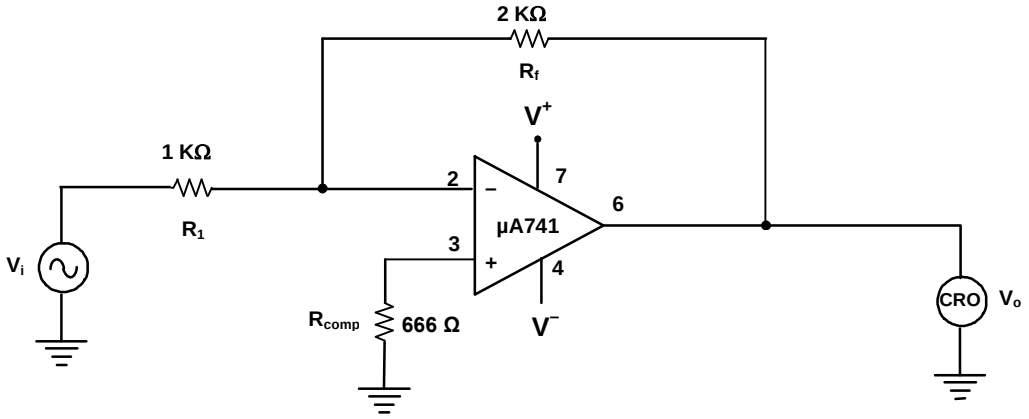


Figure1.1 Inverting amplifier

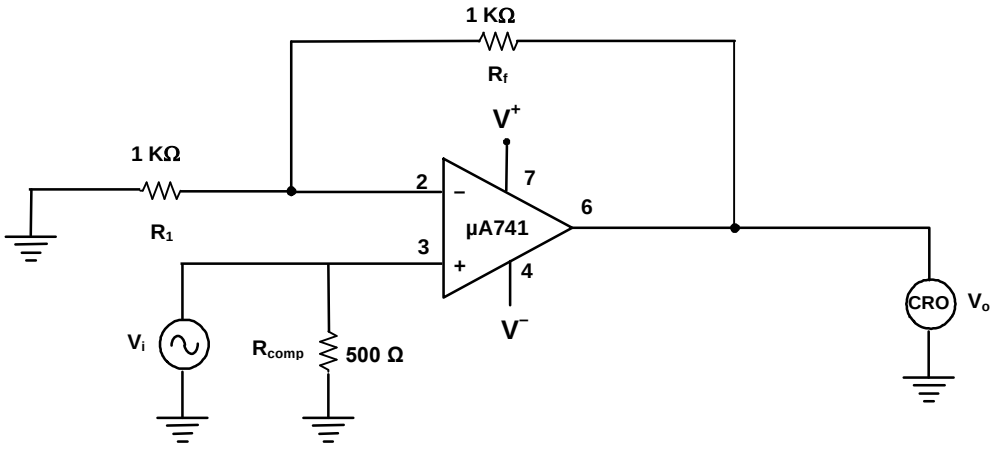


Figure1.2 Non-Inverting Amplifier

PROCEDURE:

1. The circuit connections are made as per the circuit diagram.
2. The power supply is switched ON.
3. Input signal amplitude is set to a particular value.
4. The output voltage is noted down for different values of frequency.
5. Determine the gain in dB using the formula

$$Gain = 20\log\frac{V_o}{V_i}$$

6. Draw the frequency response curve using the input frequency and gain in dB.

RESULT:

Thus the inverting and non-inverting amplifier is designed and frequency response is drawn.

VIVA QUESTIONS:

1. What is an op-amp?
2. Give the characteristics of an ideal op-amp:
3. How a non-inverting amplifier can be courted into voltage follower?
4. What is the necessity of negative feedback?
5. What are 4 building blocks of an op-amp?
6. What is the purpose of shunting C_f across R_f and connecting R_1 in series with the input signal?
7. What are the applications of Differentiator?
8. What do you mean by unity gain bandwidth?
9. What did you observe at the output when the signal frequency is increased above f_a?
10. How would you eliminate the high frequency noise in integrator?
11. What are the main applications of the Integrator?
12. Is it possible to design an analog computer using integrator and differentiator?
13. What happens to the output of integrator when input signal frequency goes below f_a?

Expt. No: 8	INSTRUMENTATION AMPLIFIER
Date:	

OBJECTIVE:

To design and study the characteristics of the instrumentation amplifier using OP-AMP.

EQUIPMENTS/COMPONENTS REQUIRED:

S.No	Equipments/Components required	Range	Quantity
1	Operational Amplifier IC	µA 741	2
2	Resistors	4.7 KΩ	2
		10 KΩ	2
		20 KΩ	1
3	Potentiometer	10 KΩ	1
4	Regulated Dual power supply	(0 – 30) V	1
5	Multimeter	-	1

THEORY:

Industrial and consumer applications, it is necessary to measure and control physical quantities. A transducer helps to measure physical quantities. The output of a transducer needs to be amplified so that it can drive an indicator or display system. The instrumentation amplifier does this amplification. The important merits of instrumentation amplifier are high gain accuracy and high gain stability with low temperature coefficient and low output impedance.

The instrumentation amplifier is composed of 3 op-amps. These are arranged so that there is one op-amp to buffer each input (+, −), and one to produce the desired output with adequate impedance matching for the function. The rightmost amplifier, along with the resistors labeled R_1 and R_2 is just the standard differential amplifier circuit, with gain = R_2/R_1. The two amplifiers on the left are the buffers. A potentiometer can be used for R, providing easy changes to the gain of the circuit. The buffer gain could be increased by putting resistors between the buffer inverting inputs and ground to shunt away some of the negative feedback.

The output voltage, V_0 is,

$$V_0 = \frac{R_2}{R_1}\left(1+2\frac{R'}{R}\right)(V_1 - V_2)$$

DESIGN:

Assume R_1 = 10 KΩ, R_2 = 20 KΩ, R' = 4.7Ω, Gain = 10

$$\frac{R_2}{R_1}\left(1+2\frac{R'}{R}\right)=10 \qquad R = 2.35\ K\Omega$$

PROCEDURE:

1. The circuit connections are made as per the circuit diagram.
2. The potentiometer resistance is measured and adjusted to say 2.4 K**Ω,** so that the gain is 10.52.
3. The input voltages V_1 & V_2 are applied to the non-inverting terminals of the op-amps and the corresponding output voltage is measured using a multimeter.
4. The procedure is repeated for several values of V_1 and V_2.
5. The output voltage V_o is compared with the theoretical value, using the formula.

$$V_o = \frac{R_2}{R_1}\left(1+2\frac{R'}{R}\right)(V_1 - V_2)$$

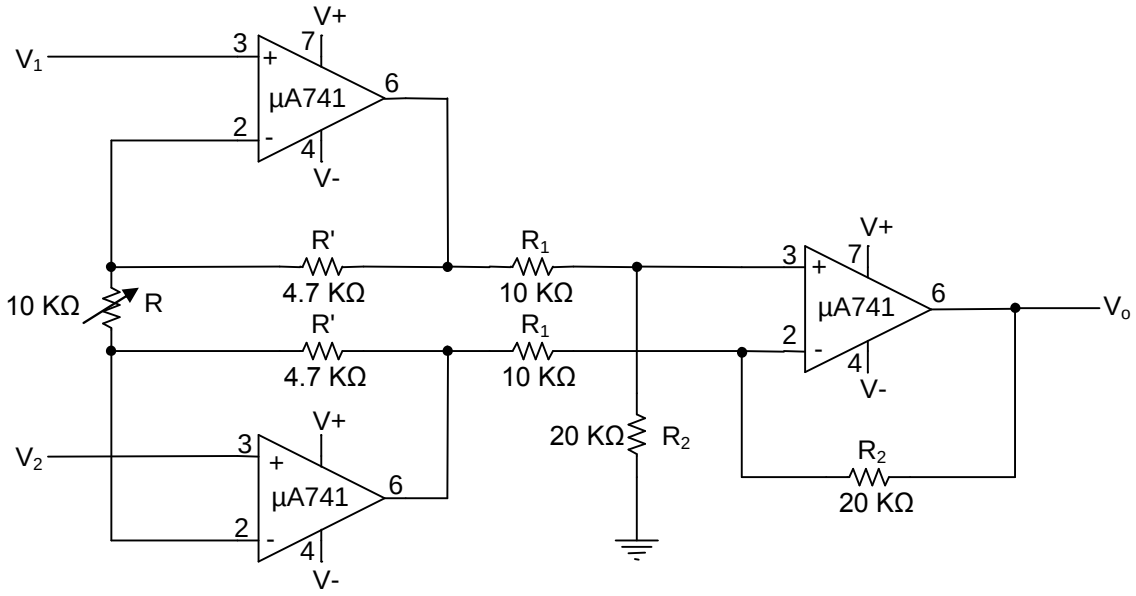


Figure 2.1: Circuit diagram of Instrumentation amplifier

TABULATION:

R = 2.35 KΩ (Constant)

V_1 (volts)	V_2 (volts)	V_o theoretical (volts)	V_o practical (volts)

V_1 = 1 V, V_2 = 0.5 V (CONSTANT)

R (KΩ)	V_o theoretical (volts)	V_o practical (volts)

RESULT:

The instrumentation amplifier is designed and the practical and theoretical values of the output voltages are verified.

VIVA QUESTIONS:

1. What do you mean by a linear IC?
2. What are applications of op-amp?
3. What are the ideal characteristics of op-amp?
4. What are the basic building blocks of op-amp?

Expt. No: 9	SECOND ORDER ACTIVE LOW AND HIGH PASS FILTERS
Date:	

OBJECTIVE:

To design second order active high pass and low pass filters and plot their frequency response.

EQUIPMENTS/COMPONENTS REQUIRED:

S.No	Equipments/Components required	Range	Quantity
1	Operational Amplifier IC	µA 741	2
2	Resistors	8 KΩ	2
		17 KΩ	1
		10 KΩ	1
3	Capacitor	0.01 µF	2
4	Regulated Dual power supply	(0 – 30) V	1
5	Multimeter	-	1
6	Function Generator	(0 – 3) MHz	1
7	Cathode Ray Oscilloscope	(0 – 30) MHz	1

THEORY:

A filter is a device that passes electric signals at certain frequencies or frequency ranges while preventing the passage of others. At high frequencies (> 1 MHz), all of these filters usually consist of passive components such as inductors (L), resistors (R), and capacitors (C). They are then called LRC filters. In the lower frequency range (1 Hz to 1 MHz), however, the inductor value becomes very large and the inductor itself gets quite bulky, making economical production difficult. In these cases, active filters become important. Active filters are circuits that use an operational amplifier as the active device in combination with some resistors and capacitors to provide an LRC-like filter performance at low frequencies.

A second order filter consists of two R-C pairs and has a roll off rate of -40 dB/decade. From the frequency response, for different values of α it may be seen that for a heavily damped filters the response is stable. If α is reduced too much the filter becomes oscillatory. The flattest pass band occurs for a damping co – efficient of 1.414.

DESIGN:

Second order LPF

Transfer function of LPF is given by

$$H(s)=\frac{A_v}{s^2C\ R\ +sCR(3-A_v)+1}$$

$$H(s)=\frac{A_v\omega_h^2}{s^2+\alpha\omega_h s+\omega_h^2}$$

$$\omega_h=\frac{1}{RC}$$

$$2\pi f_h=\frac{1}{RC}$$

$$f_h=\frac{1}{2\pi RC}$$

$$\alpha=3-A_v$$

Design specifications:

f_h = 2 KHz, α = 1.414

$A_v = 3 - \alpha$

$= 3- 1.414$

$= 1.586$

Assume R_f = 10 KΩ

$$A_v=1+\frac{R_f}{R_i}$$

$$1.586=1+\frac{10\times10^3}{R_i}$$

$$R_i=\frac{10\times10^3}{0.586}$$

$$=17.06\times10^3\Omega$$

Assume C = 0.01μF

$$f_h=\frac{1}{2\pi RC}$$

$$R=\frac{1}{2\pi f_h C}$$

$$=\frac{1}{2\pi\times2\times10^3\times0.01\times10^{-6}}$$

$$=7.96\times10^3\Omega$$

Similarly for high pass filter.

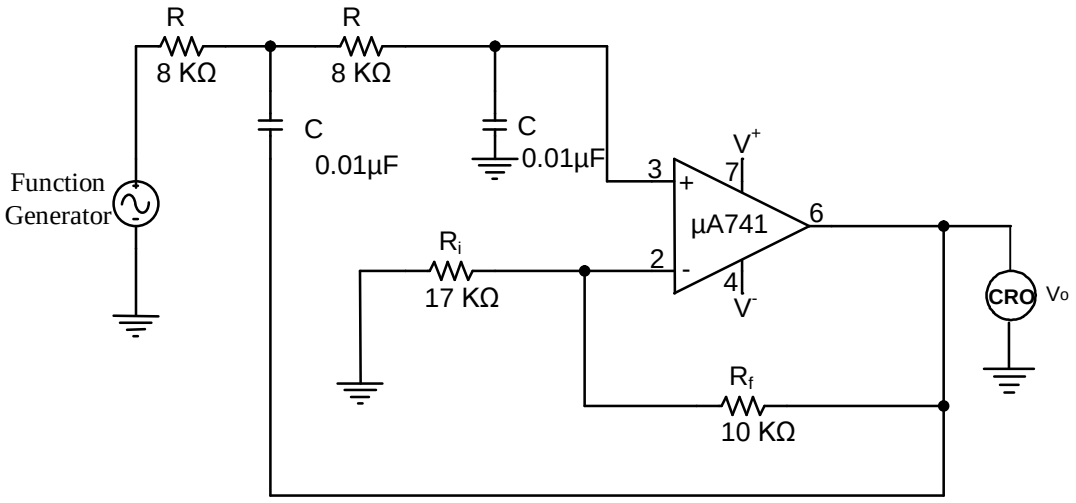


Figure 3.1. Circuit diagram of Second order low pass filter

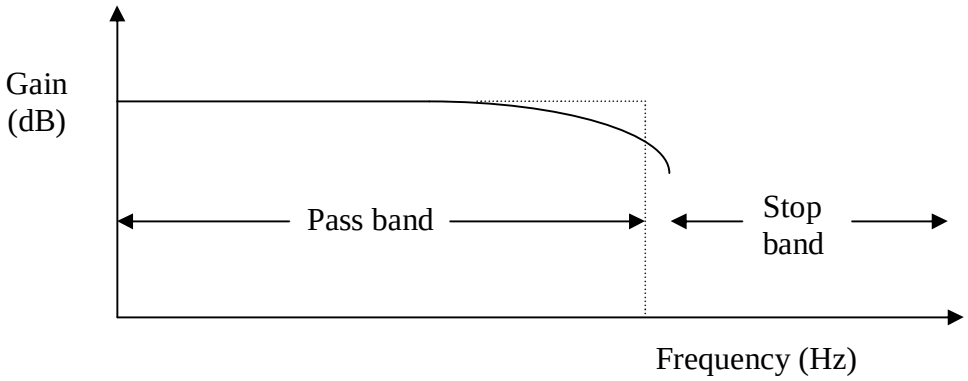


Figure 3.2. Frequency response of LPF

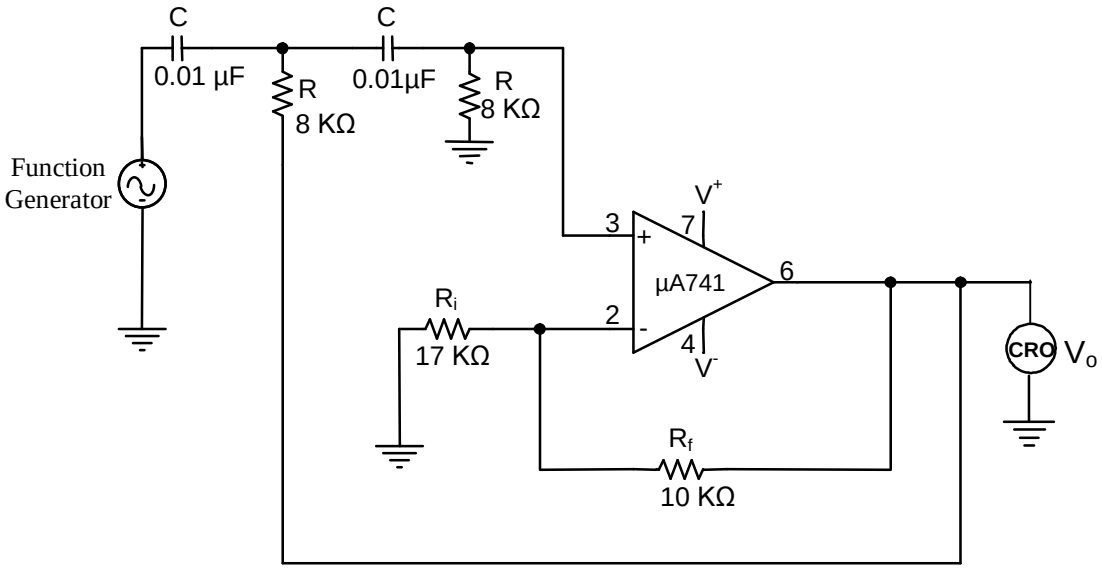


Figure 3.3. Circuit diagram of Second order high pass filter

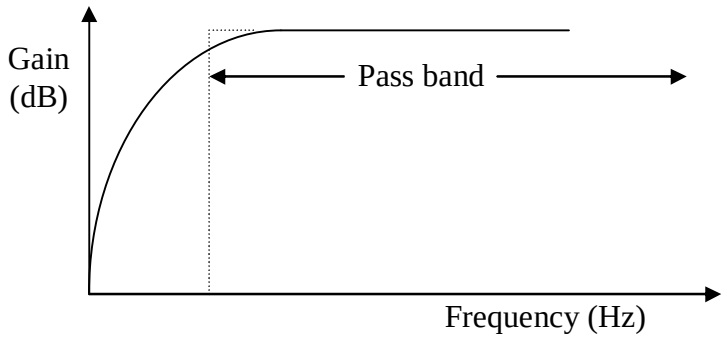


Figure3.4.Frequency response of HPF

PROCEDURE:

1. Connections are made as per the circuit diagram and the power supply is switched ON.
2. Apply the input with the signal generator and adjust the input voltage to some low value and maintain it constantly.
3. Starting from 100 Hz go on increasing the frequency and note down the output.
4. Find the gain and plot the graph.
5. Find the practical cut off frequency.

TABULATION:

Frequency (Hz)	Output Voltage (volts)	Gain = V_o/V_i	Gain in dB

RESULT:

The active second order low pass filter and high pass filter are designed and the results are

Low pass filter designed frequency =
Cut off frequency =
High pass filter designed frequency =
Cut off frequency =

VIVA QUESTIONS:

1. List the types of active filters.
2. What is the purpose of filters?
3. Define bandwidth.
4. Differentiate Band pass and band stop filter.

Expt. No: 10	PRECISION HALF & FULL WAVE RECTIFIERS
Date:	

OBJECTIVE:

To study the characteristics of precision half wave and full wave rectifier using OP AMP.

EQUIPMENTS/COMPONENTS REQUIRED:

S.No	Equipments/Components required	Range	Quantity
1	Operational Amplifier IC	µA 741	2
2	Resistors	10 KΩ	5
		20 KΩ	1
3	Diode	IN 4001	2
4	Regulated Dual power supply	(0 – 30) V	1
5	Function Generator	(0 – 3) MHz	1
6	Cathode Ray Oscilloscope	(0 – 30) MHz	1

THEORY:

Rectifier circuits are used in the design of power supply circuits. In such applications, the voltage being rectified are usually much greater than the diode voltage drop, rendering the exact value of the diode drop unimportant to the proper operation of the rectifier. In instrumentation applications, the signal to be rectified can be of very small amplitude, say 0.1 V, making it impossible to employ the conventional rectifier circuits. Also the need arises for very precise transfer characteristics. The major limitation of ordinary diode is that it cannot rectify voltages below Vy (0.6 V), the cut in voltage of the diode. A circuit that acts like an ideal diode can be designed by placing a diode in the feedback loop of an op amp. Here the cut in voltage is divided by the open loop gain of the op amp so that Vy is virtually eliminated. This circuit is called the precision diode and is capable of rectifying the input signals of the order of millivolts.

Halfwave rectifier:

During +ve half cycle of the input waveform, the op-amp inverts the input and produces -ve going output as it is applied to inverting input. Due to this –ve going output, the diode D_2 does not conduct and so the output remains zero during +ve half cycle of the input waveform. During -ve half cycle of the input waveform, the op-amp inverts the input and produces +ve going output as it is applied to inverting input. Due to this +ve going output, the diode D_2 conducts and passes the signal to the output. The direct feedback diode D_1 shunts any negative-going output back to the inverting input directly, preventing it from being reproduced.

Full wave rectifier:

During +ve half cycle of the input waveform, the first op-amp inverts the input and produces -ve going output as it is applied to inverting input. Due to this –ve going output, the diode D_2 conducts and passes the signal to the inverting input of the second op-amp which again inverts and gives out positive going signal. During -ve half cycle of the input waveform, the op-amp inverts the input and produces +ve going output as it is applied to inverting input. Due to this +ve going output, the diode D_1 conducts and pass the signal to the non-inverting input of the second op-amp and gives out positive going signal.

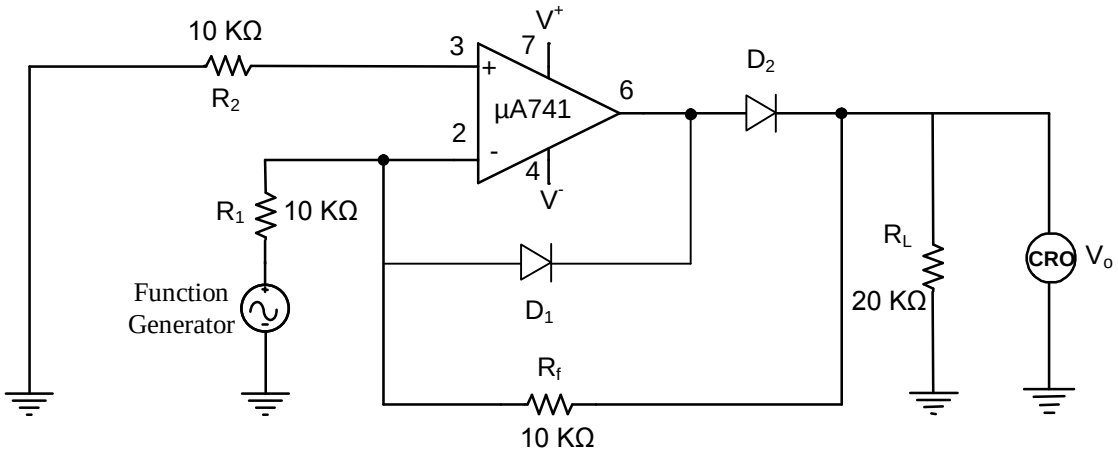


Figure 4.1 Circuit diagram of Precision Half wave rectifier

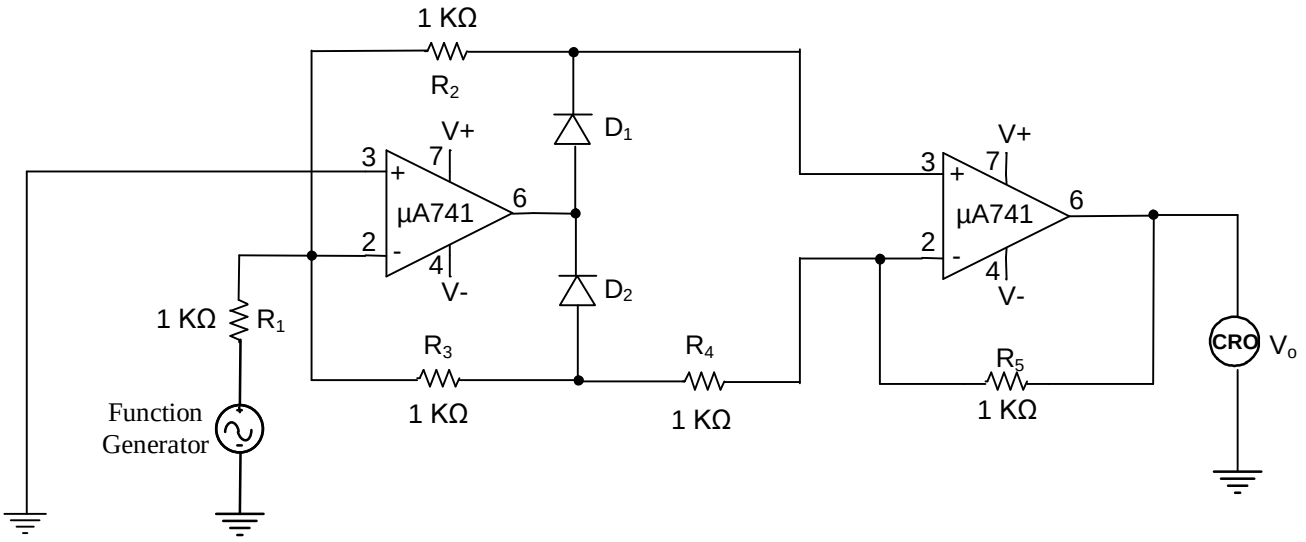


Figure 4.2. Circuit diagram of Precision Full Wave Rectifier

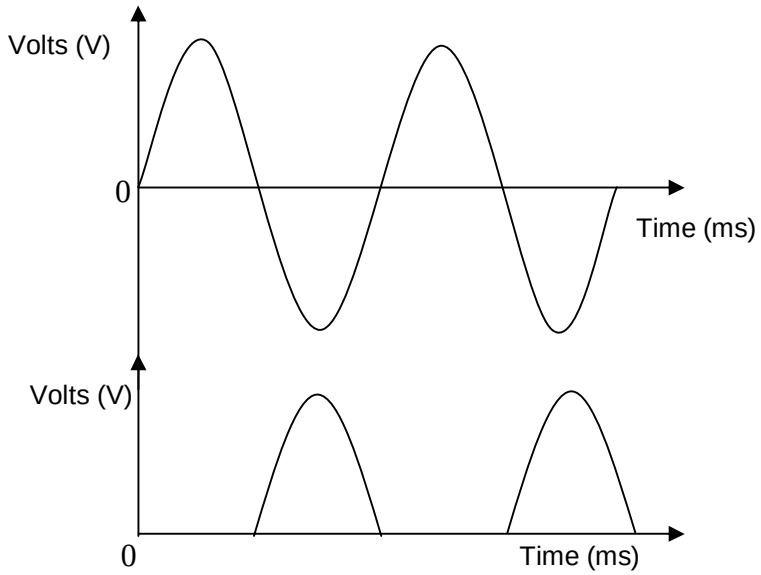


Figure 5.4. Input and Output waveform of Half-wave rectifier

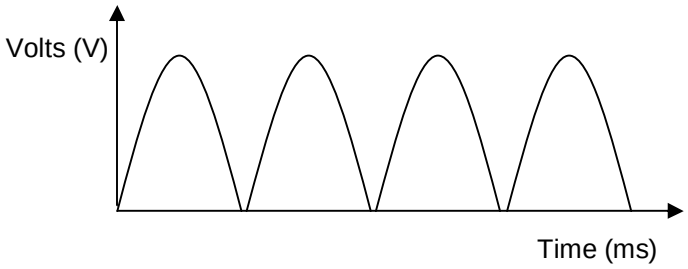


Figure 5.4. Output waveform of Full-wave rectifier

PROCEDURE:

1. Circuit connections are made as per the circuit diagram.
2. The power supply is switched ON.
3. For sinusoidal input at lower frequency from the signal generator, the rectified output waveform is observed using the CRO.
   This input waveform and the rectified waveform are plotted on the graph.

RESULT:

The characteristics of precision half wave and full wave rectifiers using op amp were studied and the graphs were drawn.

VIVA QUESTIONS:

1. Define rectifier.
2. Differentiate rectifier and inverter.
3. Define ripple factor, rectification efficiency, form factor, peak factor.

Expt. No: 11	WIEN BRIDGE OSCILLATOR
Date:	

OBJECTIVE:

To design a Wien bridge oscillator using op-amp 741 for a frequency of 1 KHz.

EQUIPMENTS/COMPONENTS REQUIRED:

S.No	Equipments/Components required	Range	Quantity
1	Operational Amplifier IC	µA 741	1
2	Resistors	16 KΩ	2
		20 KΩ	1
		10 KΩ	1
3	Potentiometer	10 KΩ	1
4	Regulated Dual power supply	(0 – 30) V	1
5	Capacitor	0.01 µF	2
6	Cathode Ray Oscilloscope	(0 – 30) MHz	1

THEORY:

Oscillator is an electronic circuit that produces a time varying or repetitive electronic signal, sine wave or square wave, without an external input signal using positive feedback. Wien Bridge Oscillator is a type of electronic oscillator that uses an RC high pass filter and an RC low pass filter for setting the frequency of oscillation while generating sine waves without any input source. The oscillator is based on a bridge circuit in the feedback which comprises of four resistors, R_1, R_2, R_3, R_4 and two capacitors, C_1, C_2. At some frequency, the reactance of the series R_1–C_1 arm will be an exact multiple of the shunt R_2–C_2 arm. If the two R_3 and R_4 arms are adjusted to the same ratio, then the bridge is balanced. Feedback is applied between the output terminal and the non inverting input terminal of the amplifier. The network produces zero phase shift at a frequency $f_o = 1/2\pi RC$ Hz. Wien bridge oscillator is the most commonly used audio frequency oscillator.

DESIGN:

$$f_o = \frac{1}{2\pi RC} Hz$$

Where $R = R_1 = R_2$ & $C = C_1 = C_2$

Assuming $C = 0.01\mu F$ & $f_o = 1$ KHz

$$R = \frac{1}{2\pi f_o C} = 15.915K\Omega \approx 16K\Omega$$

$$Gain = 1 + \left(\frac{R_4}{R_3}\right) = 3$$

So, $R_4 = 2\ R_3$

Assume R_3 = 10 KΩ, then R_4 = 20 KΩ

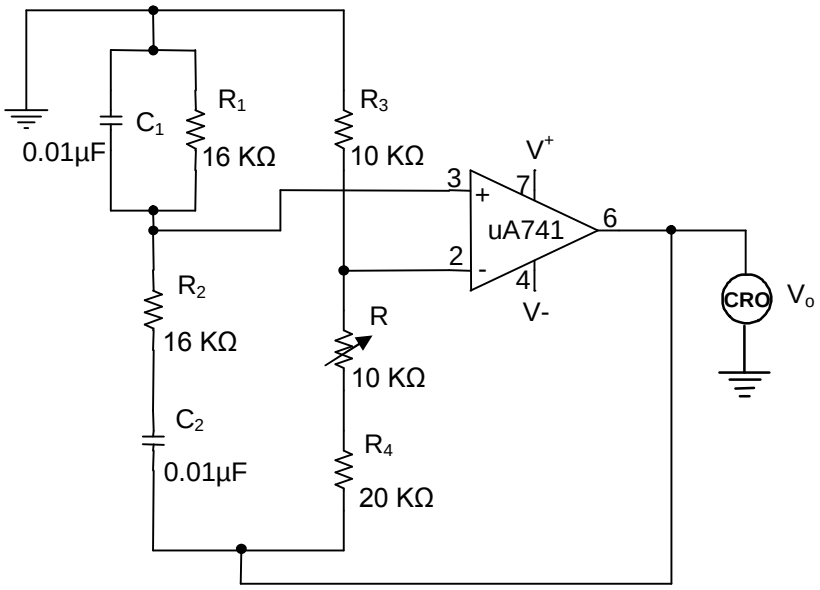


Figure 5.1. Circuit diagram of Wien bridge oscillator

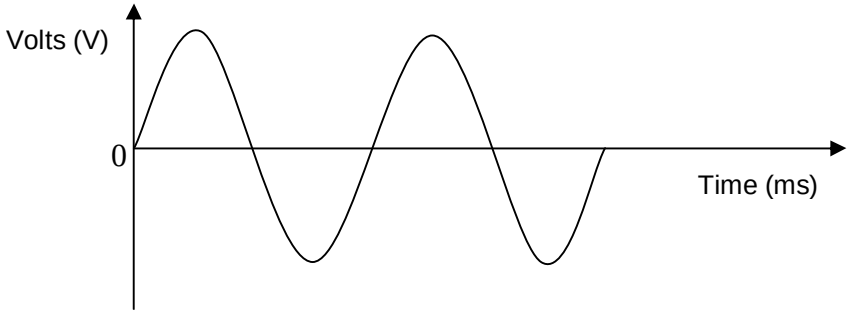


Figure 5.2 Output waveform of Wein bridge Oscillator

PROCEDURE:

1. The circuit connections are made as per the circuit diagram and the power supply is switched ON.
2. The potentiometer is adjusted to obtain the output sinusoidal waveform which is viewed using CRO.
3. The waveform is plotted on the graph.

RESULT :

Thus a Wien bridge oscillator is constructed and tested.

VIVA QUESTIONS:

1. State the two conditions for oscillations.
2. Classify the Oscillators?
3. Define an oscillator?
4. What is the frequency range generated by Wein Bridge Oscillator?
5. What is frequency stability?

Expt. No: 12 A	A. ASTABLE MULTIVIBRATORS
Date:	

OBJECTIVE:

To design Astable Multivibrators using NE555 timer IC and plot its waveforms.

EQUIPMENTS/COMPONENTS REQUIRED:

S.No	Equipments/Components required	Range	Quantity
1	Operational Amplifier IC	µA 741	1
2	Resistors	11.6 KΩ	1
		10 KΩ	2
3	Capacitor	0.05 µF	1
4	Regulated Dual power supply	(0 – 30) V	1
5	Cathode Ray Oscilloscope	(0 – 30) MHz	1

THEORY:

A 555 timer is a highly stable device for generating accurate time delay or oscillation. It can provide time delay ranging from microseconds to hours. A 555 timer can be used with supply voltage in the ranges of +5V to +18V and can drive load upto 200 mA. An astable multi vibrator or free running multi vibrator generates square waves of its own i.e. without any external excitation. It has no stable state but has only two quasi stable states between which it keeps on oscillating on its own.

In using NE 555 in astable multivibrator, the timing resistor is split into two resistors R_A and R_B. Pin 7 of discharging transistor Q_1 is connected to the junction of R_A and R_B. Initially when the output is high capacitor C starts charging towards V_{cc} through R_A and R_B. However as soon as the voltage across the capacitor equals 2/3 V_{cc} , comparator1 triggers the flip-flop and the output switches to low state. Now capacitor C discharges through R_B and the transistor Q1. When voltage across C equals 1/3 V_{cc}, comparator 2's output triggers the flip-flop and the output goes high. Then the cycle repeats. The capacitor is periodically charged and discharged between 2/3 V_{cc} and 1/3 V_{cc} respectively. The time during which the capacitor charges from 1/3 V_{cc} to 2/3 V_{cc} is equal to the time the output remains high and is given by

$$t_c = 0.693(R_A + R_B)C$$

where R_A and R_B are in ohms and C is in Farads. Similarly the time during which the capacitor discharges from 2/3 V_{cc} to 1/3 V_{cc} is equal to the time the output is low and is given by

$$t_d = 0.693R_BC$$

Thus the total time period of the output waveform is $T = t_c + t_d = 0.693(R_A + 2R_B)C$

Therefore the frequency of oscillation

$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

The output frequency, f is independent of the supply voltage V_{cc}.

DESIGN:

R_A=10 KΩ, R_B = 2.2 KΩ, C = 0.1μF & V_{cc} = 5V

$$F = \frac{1.45}{(R_A + R_B)C}$$

$$= \frac{1.45}{(10+10)\times 10^3 \times 0.1\times 10^{-6}}$$

$$= 0.725\times 10^3$$

$$= 725Hz$$

$T_{(Charging)}$ $= 0.69(R_A+R_B)\ C$

$= 0.69(10+10)\ X\ 0.1\ X\ 10^3\ X\ 10^{-6}$

$= 0.69$ msec

$T_{(Discharging)}$ $= 0.69\ R_BC$

$= 0.69\ X\ 10\ X\ 10^{-3}\ X\ 0.1\ X\ 10^{-6}$

$= 0.69$ msec

$$\text{Duty cycle} = \frac{R_B}{R_A + R_B}\times 100$$

$$= \frac{10}{10+10}\times 100$$

$$= 50\%$$

CIRCUIT DIAGRAM:

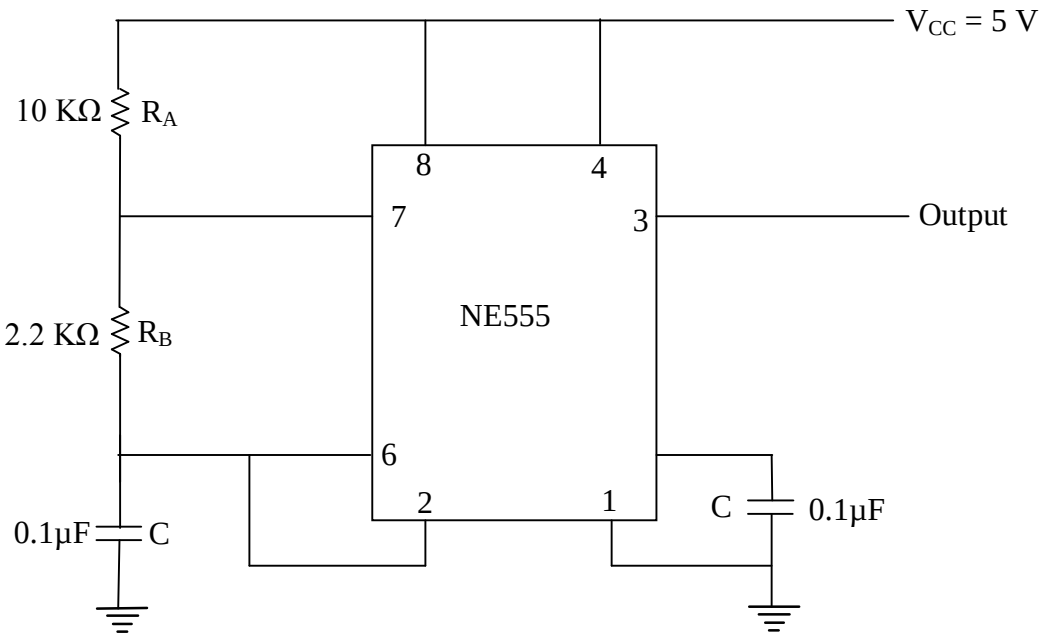
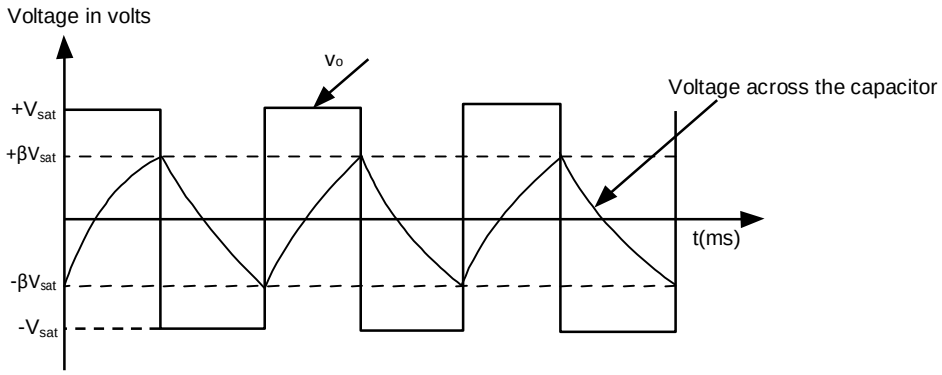


Figure.6.1 Circuit diagram of Astable Multivibrator

MODEL GRAPH:



TABULATION:

Frequency (Hz)	Output Voltage (volts)	Gain = V_o/V_i	Gain in dB

PROCEDURE:

1. Make the connections as shown in the circuit diagram
2. Keep the CRO channel switch in ground and adjust the horizontal line on the x axis so that it coincides with the central line.
3. Select the suitable voltage sensitivity and time base on the CRO.
4. Check for the correct polarity of the supply voltage to op-amp and switch on power supply to the circuit.
5. Observe the waveform at the output and across the capacitor. Measure the frequency of oscillation and the amplitude. Compare with the designed value.
6. Plot the Waveform on the graph.

RESULT:

Thus Astable Multivibrator was designed using op-amp and the waveforms were plotted.

VIVA QUESTIONS:

1. Define Multivibrator.
2. Name the types of Multivibrator**.**
3. Differentiate the types of multivibrators.

Expt. No: 12 B	B. SCHMITT TRIGGER
Date:	

OBJECTIVE:

To design and test the Schmitt trigger using Op-amp.

EQUIPMENTS/COMPONENTS REQUIRED:

S.No	Equipments/Components required	Range	Quantity
1	Operational Amplifier IC	µA 741	1
2	Resistors	1 KΩ	1
		13 Ω	1
		10 K Ω	1
4	Regulated Dual power supply	(0 – 30) V	1
5	Cathode Ray Oscilloscope	(0 – 30) MHz	1
6	Function Generator	(0 – 3) MHz	1

THEORY:

A Schmitt trigger circuit is a fast-operating voltage-level detector. When the input voltage arrives at the upper or lower trigger levels, the output changes rapidly. The circuit operates with almost any type of input waveform, and it gives a pulse-type output.

The circuit of an op-amp Schmitt trigger circuit is shown in figure. The input voltage V_{in} is applied to the inverting input terminal and the feedback voltage goes to the non-inverting terminal. This means the circuit uses positive voltage feedback instead of negative feedback, that is, in this circuit feedback voltage aids the input voltage rather than opposing it. When the circuit is positively saturated, a positive voltage is fedback to the non-inverting input. This positive input holds the output in the high state. Similarly, when the output voltage is negatively saturated, a negative voltage is fedback to the non-inverting input, holding the output in the low state. In either case, the positive feedback reinforces the existing output state. The feedback fraction, $\beta = R_2/R_1 + R_2$.When the output is positively saturated, the reference voltage applied to the non-inverting input is $V_{ref} = + \beta V_{sat}$. When the output is negatively saturated, the reference voltage is $V_{ref} = - \beta V_{sat}$. The output voltage will remain in a given state until the input voltage exceeds the reference voltage for that state. For instance, if the output is positively saturated, the reference voltage is $+ \beta V_{sat}$. The input voltage v_{in} must be increased slightly above $+ \beta V_{sat}$ to switch the output voltage from positive to negative, as shown in figure. Once the output is in the negative state, it will remain there indefinitely until the input voltage becomes more negative than $- \beta V_{sat}$. Then the output switches from negative to positive.

DESIGN:

Design specifications:

V_{CC} = 12 V, V_H = 2 V, R_1= 1 KΩ

HYSTERESIS, $V_H = V_{UT} - V_{LT}$ = 2 V

$$V_{UT} = +V_{SAT}\frac{R_2}{R_1 + R_2}$$

$$V_{LT} = -V_{SAT}\frac{R_2}{R_1 + R_2}$$

Assuming $V_{UT} = V_{LT}$, $V_{sat} = 0.9\ V_{CC}$

$$V_H = \frac{2R_1V_{sat}}{R_1 + R_2} = 2$$

$$2 = \frac{2\times1\times10^3\times12.6}{1\times10^3 + R_2}$$

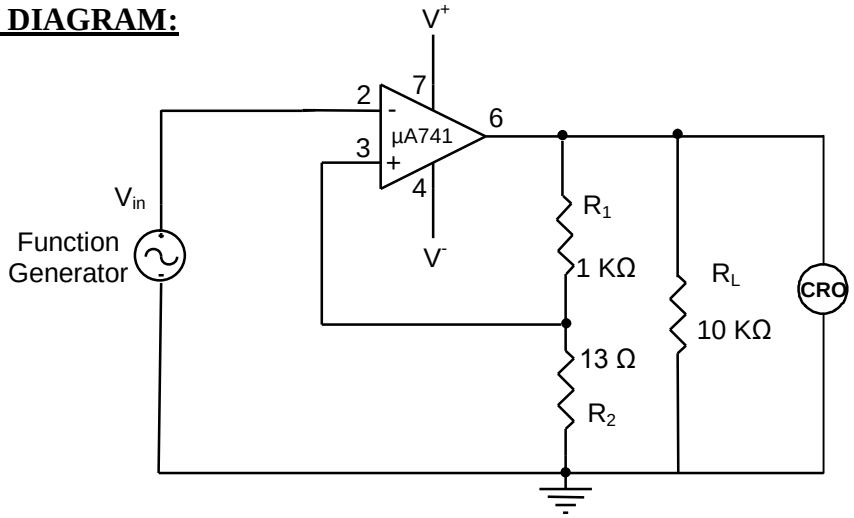
$$R_2 = 13\times10^3\Omega$$

Now

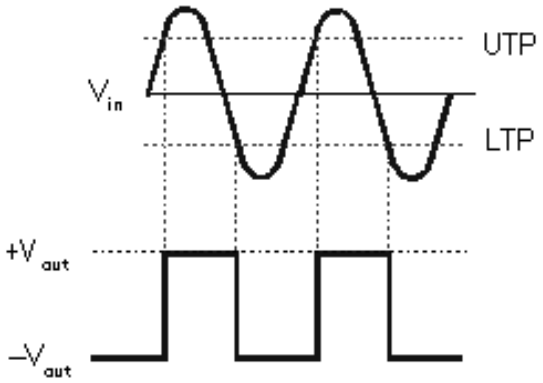
V_{UT} =

V_{HT} =

CIRCUIT DIAGRAM:



MODEL GRAPH:



PROCEDURE:

1. Connect the circuit as shown in the circuit
2. Set the input voltage as 5V (p-p) at 1KHz. (Input should be always less than V_{cc})
3. Note down the output voltage at CRO
4. To observe the phase difference between the input and the output, set the CRO in dual Mode.
5. Plot the input and output waveforms on the graph.

OBSERVATION:

Peak to peak amplitude of the output = Volts.
Frequency = Hz.
Upper threshold voltage = Volts.
Lower threshold voltage = Volts.

RESULT:

Thus Schmitt trigger using op-amp was designed & tested.

VIVA QUESTIONS:

1. What do you mean by upper and lower threshold voltage in Schmitt Trigger?
2. What is the difference between a basic comparator and the Schmitt trigger?
3. How will you produce definite Hysteresis in a Schmitt trigger using op-amp?

Expt. No: 13	DIGITAL TO ANALOG CONVERTER
Date:	

OBJECTIVE:

To design R-2R ladder type Digital to Analog Converter using op-amp.

EQUIPMENTS/COMPONENTS REQUIRED:

S.No	Equipments/Components required	Range	Quantity
1	Operational Amplifier IC	µA741	1
2	Resistor	10 KΩ	3
		20 KΩ	5
		12 KΩ	1
3	Regulated Dual power supply	(0 – 30) V	2
4	Multimeter	-	1

THEORY:

In R-2R ladder type D to A converter, only two values of resistor is used (i.e. R and 2R). Hence it is suitable for integrated circuit fabrication. The typical values of R are from 2.5 KΩ to 10 KΩ. In this output voltage is a weighted sum of digital inputs. Since the resistive ladder is a linear network, the principle of super position can be used to find the total analog output voltage for a particular digital input by adding the output voltages caused by the individual digital inputs.

DESIGN:

Output voltage, $V_o = -V_R \frac{R_f}{R}\left[\frac{b_1}{2^1}+\frac{b_2}{2^2}+\frac{b_3}{2^3}+\frac{b_4}{2^4}\right]$

Binary value = 1000 (given)
Output voltage = 6 V (given)
Reference resistor, R = 10 KΩ
Reference Voltage, V_R = 10 V
Assume, R_f = 12 KΩ
Resolution,

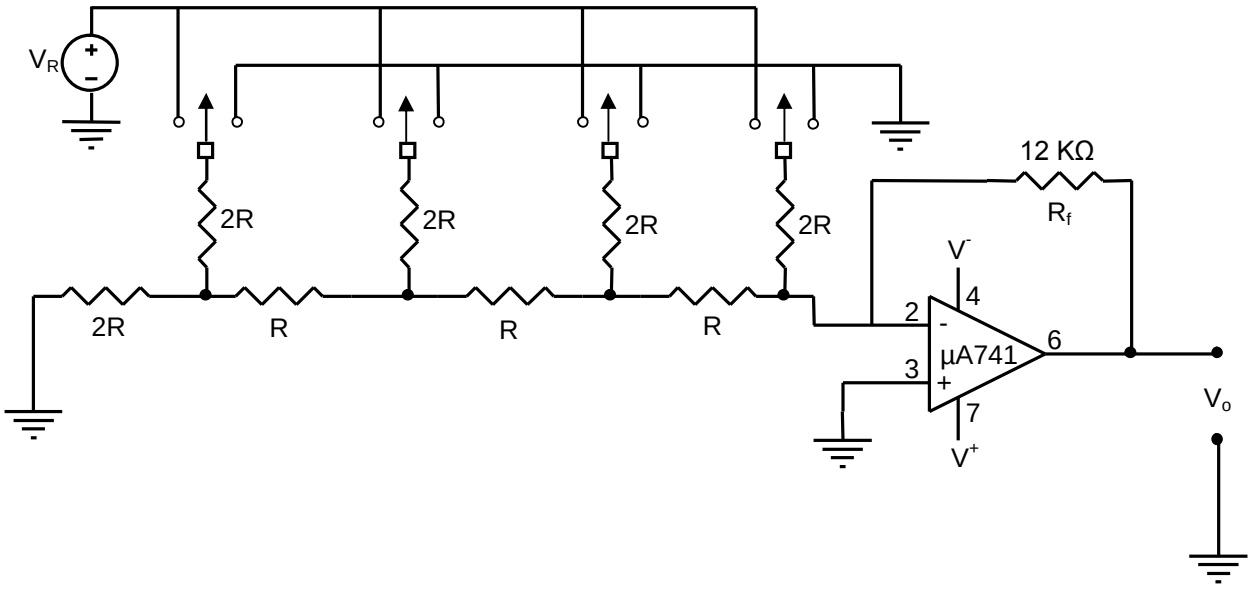
$$V = \frac{1}{2^n} \times \frac{V_R}{R} \times R_f$$

$$V = \frac{1}{2^4} \times \frac{10V}{10k\Omega} \times 12k\Omega$$

$$V = 0.75$$

CIRCUIT DIAGRAM:

4-Bit R/2R Ladder DAC:



PROCEDURE:

1. Connections are given as per the circuit diagram.
2. The power supply is switched on.
3. Reference voltage is set as 10V.
4. Binary values are applied according to the binary input values.
5. The output voltage is noted down.
6. The output voltage obtained is compared with the given output voltage.

TABULATION:

S.No	Digital binary input	Theoretical output voltage (V)	Observed output voltage (V)
1	0000		
2	0001		
3	0010		
4	0011		
5	0100		
6	0101		
7	0110		
8	0111		
9	1000		
10	1001		
11	1010		
12	1011		
13	1100		
14	1101		
15	1110		
16	1111		

RESULT:

Thus the R-2R ladder type DAC was designed using Op-amp.

VIVA QUESTIONS:

1. What is DAC**?**
2. What are the types of D to A conversion?
3. What is the output voltage of R-2R ladder network?